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Bundled ESD protection

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CeraDiode for high-speed applications

USB and Firewire are standard interfaces in computer technology and consumer electronics. Mobile phones, PDAs and control equipment used in industrial electronics are also equipped with these high-speed interfaces. Components designed to protect them against ESD are subject to special requirements because the signal integrity must not be impaired by their parasitic effects. Miniaturization and integration are additional challenges in

the development of these components.

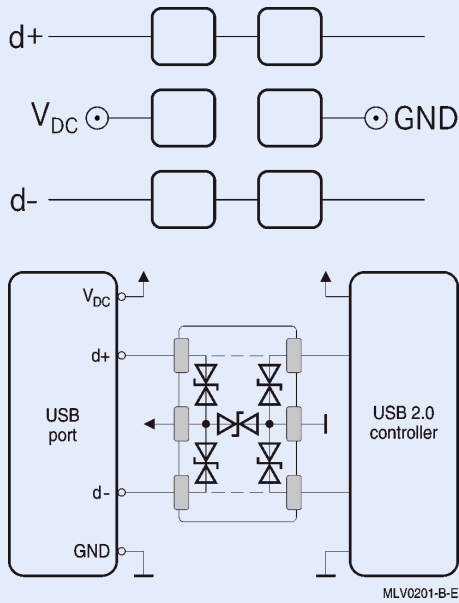
Replacement of semiconductor diodes

CeraDiodes have crucial technical advantages over semiconductor diodes. First, CeraDiodes are fundamentally bidirectional with respect to their electrical characteristics. This makes it impossible to place the component with the false polarity. Moreover, the ESD protection properties of the CeraDiode are constant up to an operating temperature of 85 °C. By comparison, the performance of semiconductor diodes begins to deteriorate already at 25 °C (temperature derating).

EPCOS has developed a new array in SOT-666 on the basis of the proven CeraDiode technology (corresponding to case size 0506). Despite its compact size, the CDA3C05GTH array accommodates no fewer than five CeraDiodes. With the new CDA3C05GTH CeraDiode Array (case size 0506, SOT-666) it is possible to protect one or two USB interfaces or one Firewire interface and save costs and space at the same time. Special value was placed on a low-capacitance design. It has a typical parasitic capacitance of <math><3\text{ pF}</math> (maximum of 5 pF), and is thus suited for high-speed data lines such as USB. Thanks to their pin-compatibility, these new components can replace SOT-666 semiconductor solutions on a 1:1 basis without having to change the layout. Figures 1 to 3 show typical applications.

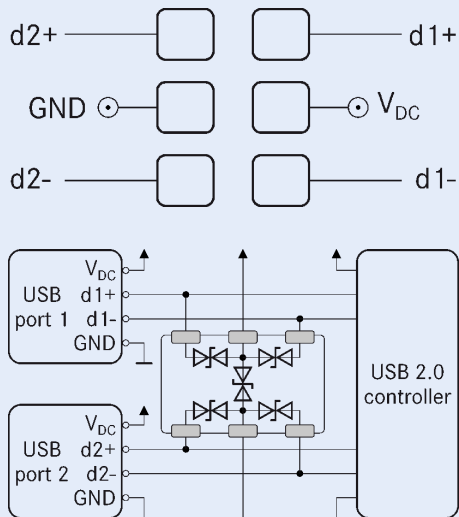
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FIGURE 1: USB 2.0 SINGLE-PORT PROTECTION



The CDA3C05GTH array has a pitch-500 design, allowing it to be placed directly onto the relevant interconnections without any special interconnection layout.

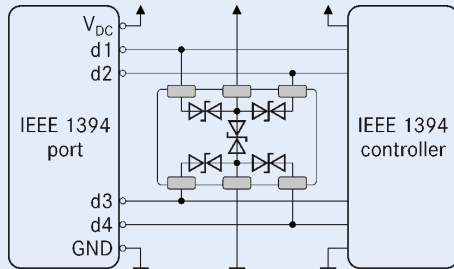
FIGURE 2: USB 2.0 DUAL-PORT PROTECTION



The new array can protect two USB ports simultaneously. It safeguards four data lines as well as the voltage supply line.

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FIGURE 3: PROTECTION OF AN IEEE 1394 PORT



In the array solution from EPCOS, a single component protects not only the four data ports but also the supply voltage of an IEEE 1394 interface (Firewire, DV) against ESD.

High ESD stability and ruggedness

The CDA3C05GTH CeraDiode array has a convincingly high ESD stability. This was confirmed by measuring the capacitance and leakage current at the data pins after stressing with ESD pulses to IEC 61000-4-2, with 8 kV contact discharge and 15 kV air discharge.

Capacitance:

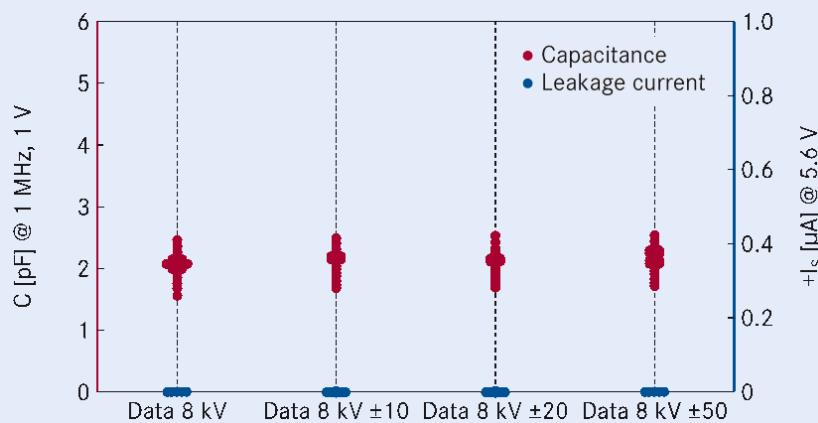
The specification stipulates that the capacitance must not exceed 5 pF after ± 10 pulses. This requirement is satisfied even after ± 100 pulses.

Leakage current:

The specification stipulates that the leakage current must not exceed 1 μA after ± 10 pulses. This requirement is completely satisfied even after ± 50 pulses.

Even after 50 ESD pulses, both the capacitance and leakage current were not only almost unchanged, but even significantly below the maximum permissible limits of 5 pF and 0.1 μA respectively. This confirms the high ESD stability and ruggedness of the component.

FIGURE 4: CHANGE OF CAPACITANCE AND LEAKAGE CURRENT WITH AN 8 KV DISCHARGE



Neither the capacitance nor the leakage current changed significantly even after 50 ESD pulses. A 15-kV test showed similar results.

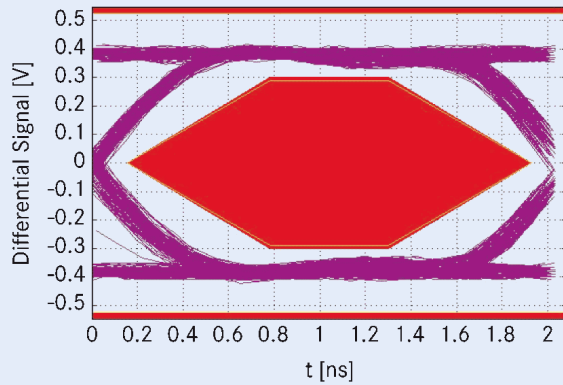
Another important selection criterion for protection components designed to protect high-speed data lines is their effect on signal integrity and the prevention of signal losses. In this context, the parasitic self-capacitance is crucial for its suitability. It must be correspondingly low to avoid impermissible flattening of the switching edges. Developers from

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EPCOS were able to reduce the self-capacitance of the individual CeraDiodes to significantly below 5 pF. The USB 2.0 compliance test confirms the suitability of the CDA3C05GTH array (Fig. 5) for this application.



FIGURE 5: EYE DIAGRAM TO USB 2.0 COMPLIANCE TEST



The signal edges must not touch the red zone – also known as the “eye.” The CeraDiode array satisfies this condition thanks to its low-capacitance design.



TABLE: OVERVIEW OF KEY ELECTRICAL PARAMETERS

Parameter	Unit	Condition	Minimum	Typical	Maximum
Max. DC operating voltage	V_{DC} [V]		-	-	5.6
Breakdown voltage	V_{BR} [V]	$I_{BR} = 1 \text{ mA}$ (any I/O pin to GND)	120	-	-
		$I_{BR} = 1 \text{ mA}$ (VDC to GND)	25	-	-
Leakage current	I_{leak} [μA]	$V_{leak} = 5.6 \text{ V}$	-	-	1
Clamping voltage	V_{clamp} [V]	$I_{PP} = 1 \text{ A}$, 8/20 μs (any I/O pin to GND)	-	-	360
		$I_{PP} = 1 \text{ A}$, 8/20 μs (VDC to GND)	-	-	72
Capacitance	C [pF]	$V = 1 \text{ V}$, $f = 1 \text{ MHz}$ (any I/O pin to GND)	-	3	5
		$V = 1 \text{ V}$, $f = 1 \text{ MHz}$ (any I/O pin to any I/O pin)	-	1.5	2.5