3 Applications

3.1 Protective circuits

The varistors must on all accounts be connected parallel to the electronic circuits to be protected.

Fig. 26a AC/DC single-phase protection

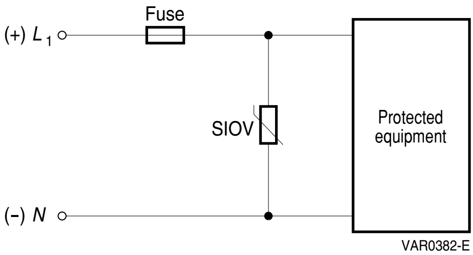
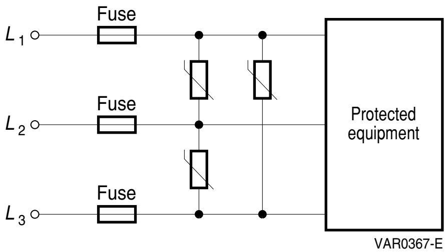


Fig. 26b AC three-phase protection



Figures 26a and b Circuit concept, power supply line-to-line protection

When varistors are used in line-to-ground circuits (figures 27a and 27b), the risk must be considered that a current type fuse may possibly not blow if the grounding resistance is too high and in this way the current is limited. With regard to such cases, various international and local standards do not allow the line-to-ground application of varistors without taking adequate safety countermeasures.

One possible solution is to use thermal fuses in series, which are thermally coupled with the varistor, as indicated in figures 27a and 27b.

Fig. 27a Single phase protection including line to ground protection

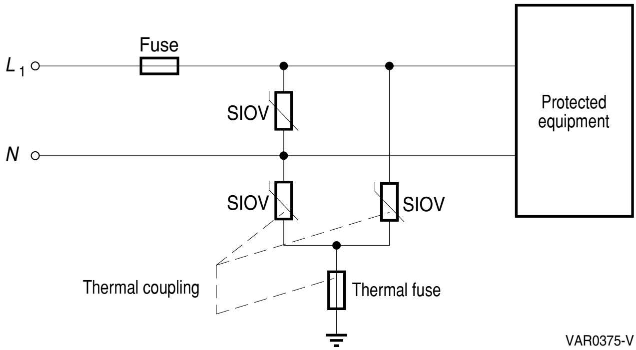
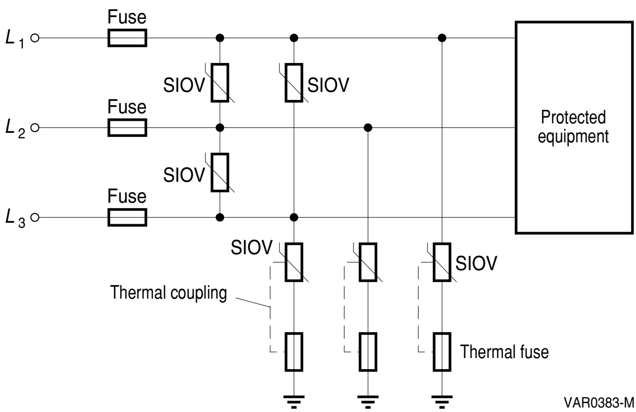
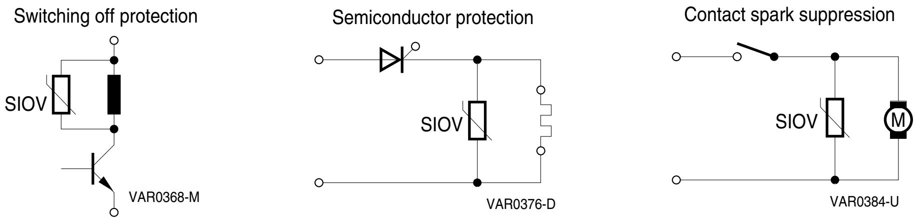


Fig. 27b Three phase protection including line to ground protection



Figures 27a and b Circuit concept, power supply line-to-ground protection



Figures 28a – c Further typical applications of varistors used as a free-wheel-circuit

3.2 CE conformity

A wide range of legislation and of harmonized standards have come into force and been published in the field of EMC in the past few years. In the European Union, the EMC Directive 89/336/EEC of the Council of the European Communites came into effect on the 1st of January 1996. As of this date, all electronic equipment must comply with the protective aims of the EMC Directive. The conformity with the respective standards must be guaranteed by the **manufacturer or importer** in the form of a declaration of conformity. A CE mark of conformity must be applied to all equipment [1].

As a matter of principle, all electrical or electronic equipment, installations and systems must meet the protection requirements of the EMC Directive and/or national EMC legislation. A declaration of conformity by the manufacturer or importer and a CE mark are required for most equipment. Exceptions to this rule and special rulings are described in detail in the EMC laws.

New, harmonized European standards have been drawn up in relation to the EEC's EMC Directive and the national EMC laws. These specify measurement techniques and limit values or severity levels, both for interference emission and for the interference susceptibility (or rather, immunity to interference) of electronic devices, equipment and systems.

The subdivision of the European standards into various categories (cf. table 3) makes it easier to find the rules that apply to the respective equipment.

The generic standards always apply to all equipment for which there is no specific product family standard or dedicated product standard.

Adherence to the standards for electromagnetic compatibility (EMC) is especially important.

These are:

- Interference emission EN 61000-6-3 and EN 61000-6-4
- Immunity to interference EN 61000-6-1 and EN 61000-6-2

[1] Kohling, Anton "CE Conformity Marking"
ISBN 3-89578-037-5, Ordering code: A19100-L531-B666

Whereas regulations concerning maximum interference emission have been in existence for some time, binding requirements concerning immunity to interference have only come into existence since 1996 for many types of equipment. In this respect, in addition to having an optimum price/performance ratio, SIOV varistors have proved themselves to be a reliable solution for all requirements concerning overvoltages:

- ESD (electrostatic discharge)
- Burst (fast transients)
- Surges, high-energy transients

The basic standards contain information on interference phenomena and general measuring methods.

The following standards and regulations form the framework of the conformity tests:

Table 3

EMC standards		Germany	Europe	International
Generic standards define the EMC environment in which a device is to operate according to its intended use				
Emission	residential	DIN EN 61000-6-3 (DIN EN 50081-1)[1]	EN 61000-6-3 (EN 50081-1)[1]	IEC 61000-6-3
	industrial	DIN EN 61000-6-4 (DIN EN 50081-2)[1]	EN 61000-6-4 (EN 50081-2)[1]	IEC 61000-6-4
Interference immunity	residential	DIN EN 61000-6-1 (DIN EN 50082-1)[1]	EN 61000-6-1 (EN 50082-1)[1]	IEC 61000-6-1
	industrial	DIN EN 61000-6-2	EN 61000-6-2	IEC 61000-6-2
Basic standards describe physical phenomena and measurement techniques				
Measuring equipment		DIN VDE 0876-16-1		CISPR 16-1
Measuring methods	emission	DIN VDE 0877-16-2		CISPR 16-2
	interference immunity	DIN EN 61000-4-1	EN 61000-4-1	IEC 61000-4-1
Harmonics		DIN EN 61000-3-2	EN 61000-3-2	IEC 61000-3-2
Flicker		DIN EN 61000-3-3	EN 61000-3-3	IEC 61000-3-3
Interference immunity parameters e. g.	ESD	DIN EN 61000-4-2	EN 61000-4-2	IEC 61000-4-2
	EM fields	DIN EN 61000-4-3	EN 61000-4-3	IEC 61000-4-3
	Burst	DIN EN 61000-4-4	EN 61000-4-4	IEC 61000-4-4
	Surge	DIN EN 61000-4-5	EN 61000-4-5	IEC 61000-4-5

1) The standards given in parentheses are previous ones, which will remain valid for a transition period.

Table 3 (continued)

EMC standards		Germany	Europe	International
Product family standards define limit values for emission and susceptibility				
ISM equipment	emission interference immunity	DIN EN 55011 [1]	EN 55011 [1]	CISPR 11 [1]
Household appliances	emission interference immunity	DIN EN 55014-1 DIN EN 55014-2	EN 55014-1 EN 55014-2	CISPR 14-1 CISPR 14-2
Lighting	emission interference immunity	DIN EN 55015 DIN EN 61547	EN 55015 EN 61547	CISPR 15 IEC 1547
Radio and TV equipment	emission interference immunity	DIN EN 55013 DIN EN 55020	EN 55013 EN 55020	CISPR 13 CISPR 20
High-voltage systems	emission	DIN VDE 0873	—	CISPR 18
ITE equipment	emission interference immunity	DIN EN 55022 DIN EN 55024	EN 55022 EN 55024	CISPR 22 CISPR 24
Vehicles	emission interference immunity	DIN VDE 0879-2 —	[2] [2]	CISPR 25 ISO 11451 ISO 11452

The following table shows the most important standards in the field of immunity to interference.

Standard	Test characteristics	Phenomena
Conducted interference		
EN 61000-4-4 IEC 61000-4-4	5/50 ns (single pulse) 2,5 or 5 kHz burst	Burst Cause: switching processes
EN 61000-4-5 IEC 61000-4-5	1,2/50 µs (open-circuit voltage) 8/20 µs (short-circuit current)	Surge (high-energy transients) Cause: lightning strikes mains lines, switching processes
EN 61000-4-6 (ENV 50141) IEC 61000-4-6	1 V, 3 V, 10 V 150 kHz to 80 MHz	High-frequency coupling Narrow-band interference
Radiated interference		
EN 61000-4-3 (ENV 50140) IEC 61000-4-3	3 V/m, 10 V/m 80 to 1000 MHz	High-frequency interference fields

1) Is governed by the safety and quality standards of the product families.
2) The EU Automotive Directive (95/54/EC) also covers limits and interference immunity requirements.

Table 3 (continued)

Standard	Test characteristics	Phenomena
Electrostatic discharge (ESD)		
EN 61000-4-2 IEC 61000-4-2	Up to 15 kV figure 29	Electrostatic discharge

The IEC 61000 or EN 61000 series of standards are planned as central EMC standards into which all EMC regulations (e.g. IEC 60801, IEC 60555) are to be integrated in the next few years.

3.3 ESD

3.3.1 Standard IEC 61000-4-2

The trend to ever smaller components and lower and lower signal levels increases the susceptibility of electronic circuits to interference due to electrostatic disturbances. Simply touching the device may lead to electrostatic discharge causing function disturbances with far-reaching consequences or to component breakdown. Studies have shown that the human body on an insulated ground surface (e. g. artificial fiber carpeting), can be charged up to 15 kV.

In order to safeguard the immunity to interference and thus ensure CE conformity, measures are needed to prevent damage due to **e**lectro**s**tatic **d**ischarge (ESD). This applies to both the circuit layout and to selection of suitable overvoltage protection.

IEC 61000-4-2 describes the test procedures and specifies severity levels:

Figure 29 shows the discharge circuit, figure 30 the waveform of the discharge current with an extremely short rise time of 0,7 to 1,0 ns and amplitudes of up to 45 A. Secondary effects caused by this edge steepness are high electrical and magnetic fields strengths.

In the ESD test, at least 10 test pulses of the polarity to which the device under test is most sensitive are applied.

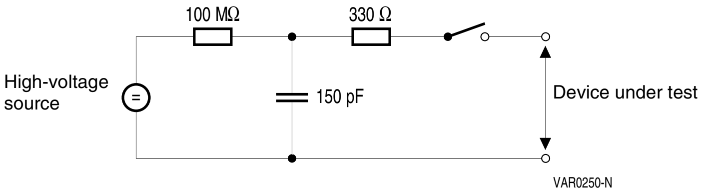


Figure 29 ESD discharge circuit according to IEC 61000-4-2

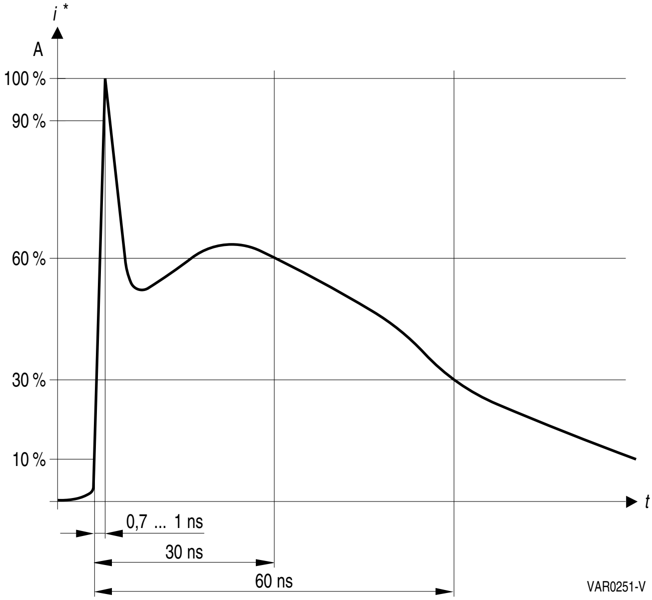


Figure 30 ESD discharge current according to IEC 61000-4-2

For these reasons, suitable overvoltage protection elements must meet the following requirements:

- response time < 0,5 ns
- bipolar characteristics
- sufficient surge current handling capability
- low protection level

In addition, the following requirements are desirable:

- smallest possible component size
- SMD design
- stable capacitance values for RF interference suppression, or also low capacitance values for systems with high-speed data transmission rates, respectively
- wide operating voltage range
- high operating temperature

3.3.2 Multilayer varistors for all ESD protection requirements

EPCOS multilayer chip varistors (MLV) have been used successfully since more than 10 years in a wide field of applications. During this time they have become the most popular component for ESD protection. In the cellular phone industry multilayer varistors represent meanwhile the worldstandard in ESD protection.

Very fast response time and reliable ESD absorption capability over a broad operating temperature range at small sizes (0402 to 2220) made SIOV-MLVs become the first choice in the electronic industry.

Field rejects caused by ESD sensitivity of a device are expensive and may affect the success of the end product. Another important fact is the susceptibility of the components used in the design.

The advanced semiconductor technology of the recent years has created a very small geometry inside the components which is very sensitive to any kind of EM-interference. The integration of additional features in applications like cellular phones lead to an increasing number of components. On the other side less board space is available due to the trend of miniaturization of the whole product. As a consequence smaller components are required. Excessive noise levels caused by EMI (Electro Magnetic Interference) or RFI (Radio Frequency Interference) can impair the proper operation and the reliability of the design. Unwanted transients, like ESD spikes, coming through the I/O-ports of your device may lead to memory losses and/or IC destruction.

Next to the MLV-standard range EPCOS offers types designed for telecom line protection, automotive applications and special parts with defined capacitance tolerances, which can be used additionally to enable a device to comply with other EMC standards. EPCOS has developed varistor arrays which provide reliable ESD protection of 4 data lines in a 0612 package only.

3.3.3 Principle of ESD protection

The following aspects must be taken into consideration when designing ESD protection circuits:

Provision of an alternative current path

Figure 31 illustrates the principle involved. The protective element must have the electrical characteristics required for effective ESD protection as specified in chapter 3.3.1.

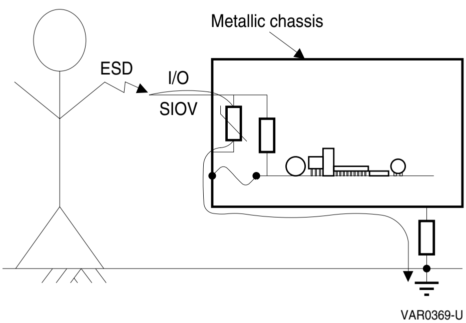


Figure 31 Alternative current path for draining an ESD pulse

Shielding

The extremely steep leading edges of short electrostatic discharge pulses induce strong electromagnetic fields which should be contained, i.e. shielded by metal casings or other measures.

Circuit board layout

The following criteria must be observed when designing PCB layouts:

- Minimize the trace length.
- Keep the suppressor conductor paths and lead lengths to an absolute minimum.
- The varistor should be placed as close to the input terminals or connectors as possible.
- Avoid running protected conductors in parallel with unprotected conductors.
- Never run critical signals (clocks, resets, etc.) near card edges. These areas are especially sensitive to induced ESD voltages.
- Minimize all conductive loops, including power and ground loops.
- The ESD transients return path to ground should be kept as short as possible, and shared transient return paths to a common ground point should be avoided.
- Use ground planes whenever possible.

3.3.4 Susceptibility of semiconductors

Almost all up-to-date ICs are protected by an integrated low-power ESD protection. This is designed to prevent ESD damage in the course of handling and component placement. Figure 32 shows typical discharge susceptibility values, which are always higher than 100 V within the time range of ESD impulses.

Device type	Static discharge susceptibility (V)
MOSFET	100– 200
GaAs FET	100–1000
EPROM	100
JFET	140–7000
CMOS	250– 300
Film Resistors	300–3000

Figure 32 Susceptibility levels of semiconductors

For this reason, in most applications it is not always necessary to select the ESD protection component with the lowest possible protection level. As explained in section 2.5.1, this procedure can lead to electrical advantages (lower leakage currents, lower capacitance) and reduced costs (smaller variety of components to be kept in stock).

For example, MLVs with up to 26 V_{DC} are frequently used in mobile phones due to the above consideration, although the operating voltage of cellular phones is currently only 3–5 V_{DC}.

3.3.5 Multilayer varistors (MLV) vs. semiconductors

Response time

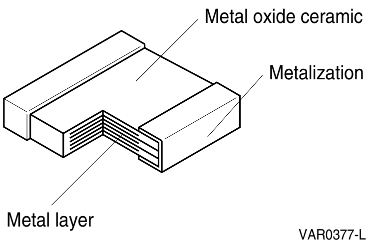


Figure 33 Structure of a multilayer chip varistor (MLV)

Figure 33 shows the structure of MLVs, which achieves extremely low parasitic inductances and permits response times of < 0,5 ns. Figure 34 shows the virtually delay-free response to a 4 kV ESD impulse.

As opposed to this, if semiconductors are used, the response time is often increased to > 1 ns because of the inductance of the cases (cf. 1.7.9).

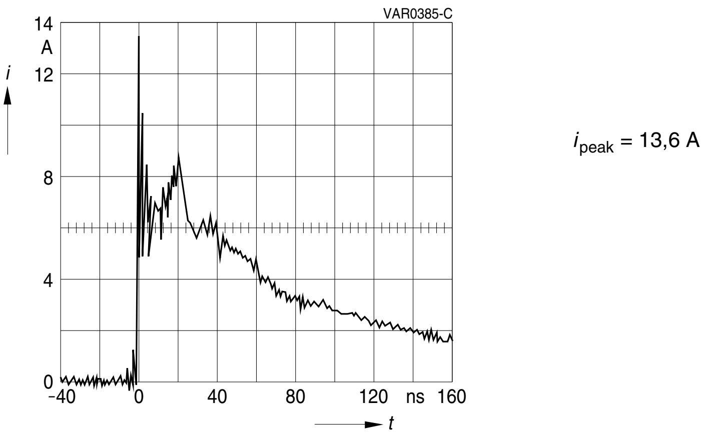


Figure 34 Response behavior to an ESD pulse (4 kV contact discharge), using SIOV-CN0603M7G as an example (current through the varistor during ESD)

Surge current handling capability

The interleaved electrode arrangement of MLVs allows surge currents of over 1 kA to be handled, whereas semiconductors can often withstand only a few amperes. This characteristic enables MLVs to be used not only for protection against ESD, but also for dealing with surge loads of much higher energy levels in accordance with IEC 61000-4-5.

Bipolar characteristics

ESD can occur with any polarity, which poses no problems for MLVs with their symmetrical protection characteristics, whereas two components are often required in order to achieve the required bipolar characteristic with semiconductors.

Operating temperatures

As shown in figure 35, MLVs can be subjected to full load at temperatures of up to 125 °C, whereas the load capacity of semiconductor components (e.g. suppressor diodes) derates from temperatures of 25 °C upwards and is frequently reduced to 25 % of the rated value at 125 °C. For compensation, an additional current-limiting resistor often has to be connected in series with semiconductor circuits.

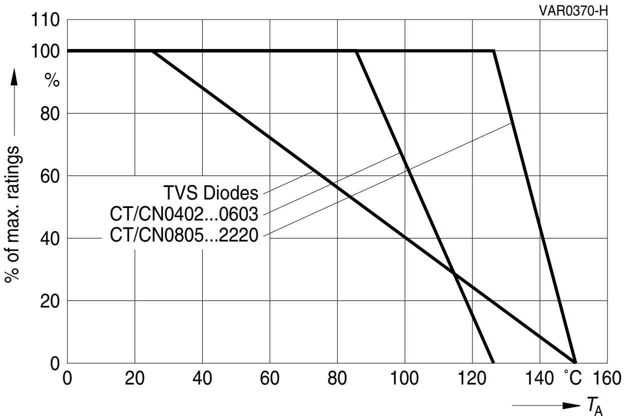


Figure 35 Temperature derating: MLV vs. transient voltage surge diodes

Size

The ceramic material of MLVs serves as an insulator on the exterior surfaces; the terminal electrodes are available as direct contact surfaces.

By comparison, semiconductor components always require a casing. This makes them correspondingly bulkier and they require more mounting space, (figure 36).

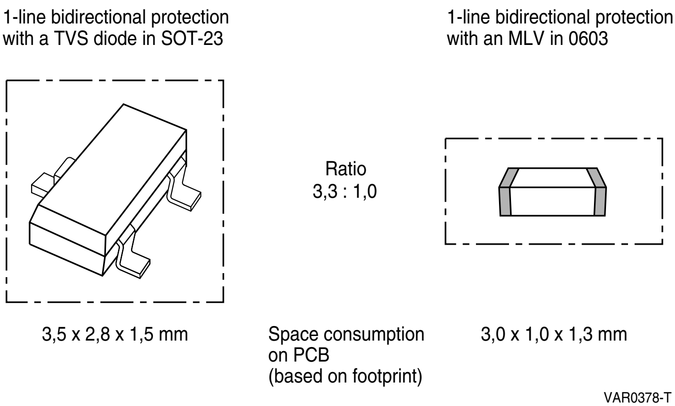


Figure 36 Space consumption: Transient voltage suppressor diode vs. MLV

3.3.6 Substitution of filter capacitors

In general for the protection of data lines it is of interest that the capacitance (also the parasitic) is kept low or within a defined range. A too large capacitance value on the signal line would influence the signal in a non-intended way.

On the other hand the EMC standards require filter elements which are able to suppress every unwanted noise signals.

To comply with those requirements EPCOS has developed special multilayer varistor types with low (LC), defined (CC) or high capacitance levels (HC).

- Low capacitance (LC), for creating a low-pass filter especially needed in high-speed data lines.
- “Controlled” capacitance (CC), to replace a capacitor for filtering purposes at I/O ports with the benefit of ESD protection plus the saving of additional chip capacitors.
- High capacitance (HC), for noise suppression (RFI, EMI) on DC lines.

The capacitance ratings listed in the product tables are typical values.

In general the following rules can be applied:

- Higher capacitance values are achieved by selecting a larger chip
- Lower capacitance values are achieved by selecting a smaller chip, or, where this is not possible, a higher voltage class.

If a specific circuit or substitution calls for defined capacitance value tolerances, then EPCOS is prepared to supply these specifically for the application as “controlled capacitance” versions.

Examples of special types with specified maximum capacitances are:

SIOV-CT0402V275RFG	$C <$ 3 pF	see 3.3.9
SIOV-CT/CN0603K17LCG	$C <$ 50 pF	see product tables
SIOV-CT/CN0805K17LCG	$C <$ 100 pF	see product tables

More details on these types and on other special designs with different capacitance and tolerance values can be supplied upon request.

3.3.7 Substitution of ESD/RFI/EMI protection circuits

Usually data line protection against ESD/RFI/EMI influence will be achieved by adapting combination circuits like shown in figure 37a.

In many cases, these components can be substituted by only one MLV varistor with defined capacitance (figure 37b). Such solutions reduce bulk and costs considerably while improving reliability. For example, as many as ten data lines in cellular phones can be protected in this way by using “controlled capacitance” MLVs.

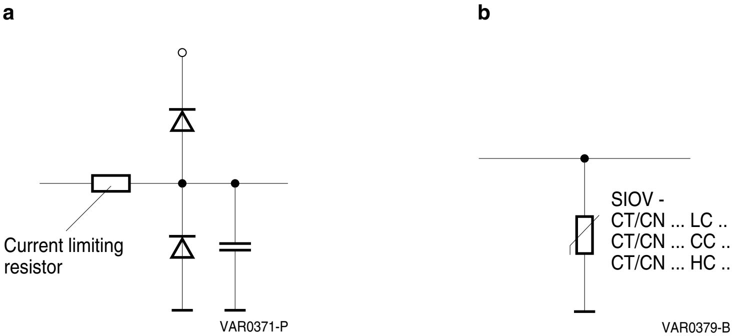
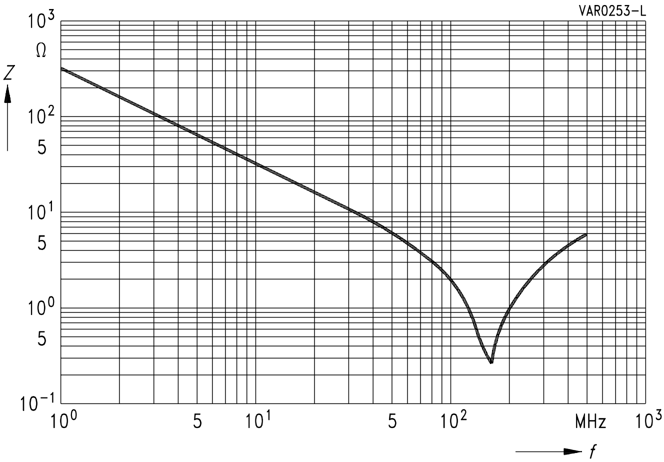


Figure 37 One MLV can replace up to four components

3.3.8 RF behavior of MLVs

Figures 38a and 38b show the typical RF behavior of multilayer varistors with a capacitance value which remains practically constant over a wide frequency range.

a



b

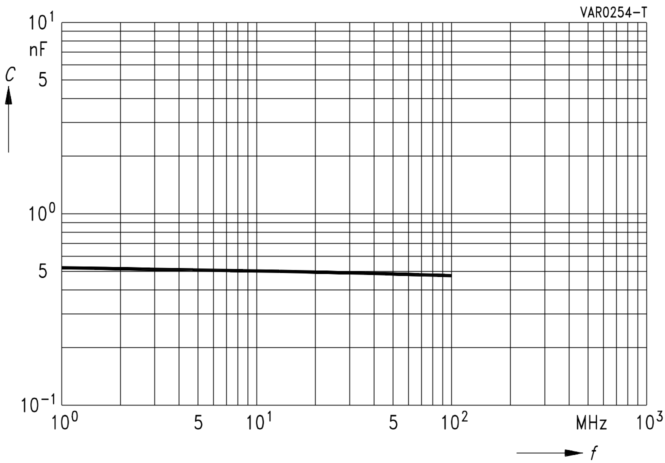


Figure 38 Typical frequency response of the impedance (a) and the capacitance (b), using the multilayer varistor SIOV-CN0805M6G as an example

3.3.9 ESD protection for antennas

ESD protection for antennas – e. g. mobile phones – requires components with ultra-low capacitance values and low insertion losses.

It is for applications such as these that EPCOS has developed an 0402-MLV with a maximum capacitance of below 3 pF, type CT0402V275RFG (figure 38c). Specifications and ordering code upon request.

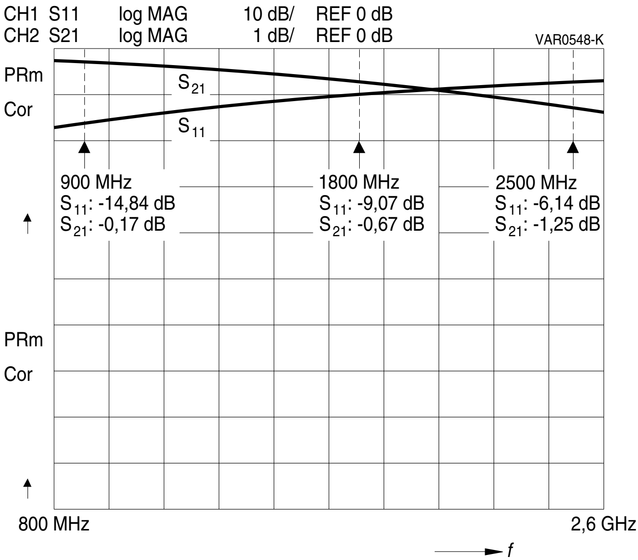


Figure 38c Typical S parameters
(including losses due to PCB and reflection)

	S11*	S21 (incl. losses of PCB)	S21 (component-matched)
900 MHz	– 14,84 dB	– 0,17 dB	– 0,1 dB
1800 MHz	– 9,07 dB	– 0,67 dB	– 0,2 dB
2500 MHz	– 6,14 dB	– 1,25 dB	– 0,4 dB

* $S11 = 20 \log \cdot \frac{SWR - 1}{SWR + 1}$

3.3.10 Typical applications for MLVs

MLVs have already come to be used for ESD/RFI/EMI protection in a wide range of applications, ref. figure 39:

- Mobile (cellular) phones, cordless phones, chargers, car kits, interface cables
- Computers, notebooks
- Automotive (airbags, keyless entry systems, car radio, ABS)
- Entertainment (I/O ports of VCR, TV sets, satellite receivers, set top boxes)
- Industrial equipment (protection of CMOS, ASIC, point of sales terminals)

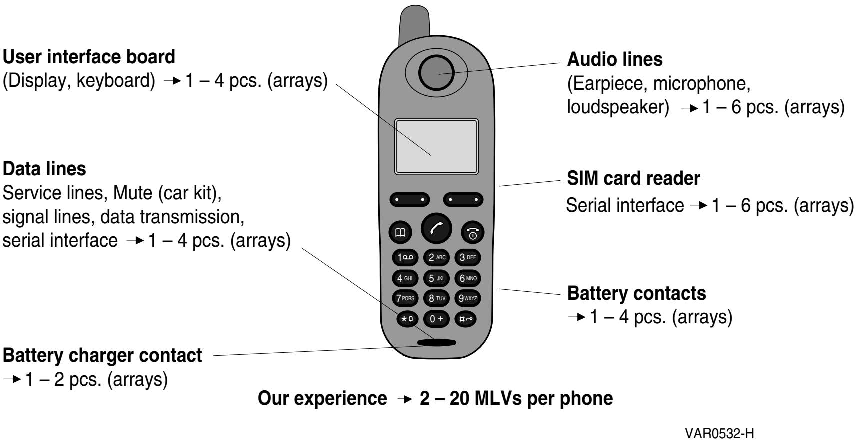


Figure 39 Application areas of MLVs, using mobile phones as an example

3.3.11 Energy of an ESD pulse

IEC 61000-4-2 specifies 15 kV as the highest charging voltage (severity level 4, air discharge) for the 150 pF discharge capacitor according to figure 29.

This means that the stored energy is

$W^* = 0{,}5 \cdot C \cdot V^2 = 0{,}5 \cdot 150 \cdot 10^{-12} \cdot 15^2 \cdot 10^6 < 0{,}02\ \mathrm{J}$

The 330-Ω resistor limits the surge current to a maximum of

$$\hat{i}^* = \frac{V^*}{R} = \frac{15\,000\ [V]}{330\ [\Omega]} \approx 45\ \mathrm{A}$$

If this surge current is to be handled by a multilayer varistor, then, according to equation 12, the effect of the varistor on this value of the current amplitude is negligible.

For CN0805M6G, for example, this means that:

$$\hat{i}^* = \frac{V_s - V_{SIOV}}{Z_{source}} = \frac{15\,000\ [V] - 45\ [V]}{330\ [\Omega]} \approx 45\ \mathrm{A}$$

By transforming the discharge current (figure 21) into an equivalent rectangular wave, we obtain $t^*_r \approx 40$ ns.

No value can be deduced from the derating curves for such an extremely short current flow time.

The energy absorption of multilayer varistors during ESD discharges lies in the region of µJ.

For the SIOV-CN0805M6G, for example, according to equation 16 this means that:

$W^* = \hat{v}^* \hat{i}^*\ t^*_r = 45 \cdot 45 \cdot 40 \cdot 10^{-9} = 80\ \mu\mathrm{J}$

Thus the largest part of the energy content of the ESD pulse is absorbed by the 330-Ω discharge resistor.

All types of the SIOV-MLV series are able to meet the (severest) ESD test level 4 acc. to IEC 61000-4-2. Figure 60 demonstrates this for multible pulses taking the CN0603M7G as an example.

Due to the steep edge of the ESD pulse, the mechanical construction of a device is of great importance for the test result. The ESD varistor selection should therefore always be verified by a test circuit.

3.4 Burst

According to IEC 61000-4-4, burst pulses are low-energy transients with steep edges and high repetition rate. Thus, for equipment to pass burst testing successfully, design (line filter, grounding concept, case) is as critical as the choice of the varistor. If IEC 61000-4-5 has been taken into account when selecting varistors, they will normally also handle the burst pulse energy without any problems. Due to the steepness of the pulse edges, the varistors must be connected in a way which keeps parasitic circuit inductance low. The EPCOS EMC laboratory will carry out tests upon request (cf. 3.7).

3.5 Surge voltages

The immunity to interference against (high-energy) surge voltages is tested in accordance with IEC 61000-4-5. The transient is generated using a combination wave (hybrid) generator.

The severity level to be applied in the immunity test must be defined as a function of the installation conditions.

In most cases, the respective product standards demand 5 positive and 5 negative voltage pulses. Standard IEC 61000-4-5 specifies severity level 4 (line-to-line, 2 kV applied via 2 Ω) as being the highest energy load. Table 4 illustrates that even the small varistor size SIOV-S10 is suitable for absorbing this energy level.

The table also shows the assessments for the other severity level. The maximum current and voltage values given have been calculated using Pspice.

Table 4 has been supplemented by the 4 kV test level. The application of this test level has proven its worth in device protection for AC power supplies (without primary protection). Even this case can be dealt with using varistors of the standard series SIOV-S20, or, in case of space limitations, by using the decreased-size EnergetiQ series SIOV-Q14.

For the immunity testing line-to-earth of power supplies, IEC 61000-4-5 specifies 12 Ω as the internal resistance of the test generator. The energy content, which is considerably lowered due to this, permits the use of the "small" type series SIOV-S05 and SIOV-S07 or the corresponding SMD versions SIOV-CU3225 or SIOV-CU4032.

For all other types of line, the internal resistance of the generator should be set to 42 Ω.

Note:
Connection of varistors to ground may be subject to restrictions. This must be clarified with the respective authorization offices.

Table 4

Application		2 Ω, 10 load cycles					
AC power supply line-to-line		230 Vrms			400 Vrms		
Severity level	kV	Type	I^*_{max} A	V^*_{max} V	Type	I^*_{max} A	V^*_{max} V
1	0,5	overvoltage protection not necessary					
2	1	S07K275 CU4032K275G2	135	820	S05K460 CU4032K460G2[1)]	3	1000
3	2	S10K275	590	920	S10K460	360	1430
4	(4)	S20K275 Q14K275	1560	900	S20K460	1300	1530

1) The electrical equivalent to the S05K460 would be a CU3225 version. Because this size is not available with 460 V rating, the (oversized) CU4032K460G2 is specified here.

3.6 Interference emission

Switching off inductive loads can lead to overvoltages which may become sources of line interference as well as of inductively and/or capacitively coupled interference. This kind of interference can be suppressed using varistors connected as a fly-wheel circuit.

SHCV varistors are especially well-suited for radio-frequency interference suppression.

3.7 EMC systems engineering

EPCOS is your competent partner when it comes to solving EMC problems.

Our performance range covers

- systems for measuring and testing EMC
- shielded rooms for EMP measures
- anechoic chambers
- EMC consultation services and planning

For further details, please refer to the *"Chokes and Inductors"* data book
(ordering no. EPC: 24003-7600).

3.8 Protection of automotive electrical systems

3.8.1 Requirements

Electronic equipment must work reliably in its electromagnetic environment without, in turn, unduly influencing this environment. This requirement, known as electromagnetic compatibility (EMC), is especially important in automotive electrical systems, where energy of mJ levels is sufficient to disturb or destroy devices that are essential for safety. EPCOS has devised a wide range of special models matched to the particular demands encountered in automotive power supplies:

- extra high energy absorption (load dump)
- effective limiting of transients
- low leakage current
- jump-start capability (no varistor damage at double the car battery voltage)
- insensitive to reverse polarity
- wide range of operating temperature
- high resistance to cyclic temperature stress
- high capacitance for RFI suppression

EPCOS automotive varistors (SIOV-…AUTO) and SHCVs suit all these demands. They are specified separately in the product tables.

3.8.2 Transients

Standard ISO 7637 (DIN 40839), details the EMC in automotive electrical systems. The toughest test for transient suppression is pulse 5, simulating load dump. This critical fault occurs when a battery is accidentally disconnected from the generator while the engine is running, e. g. because of a broken cable. Under this condition peak voltages up to 200 V can occur, lasting for few hundred ms, yielding energy levels up to 100 J. This worst case, as well as the other pulse loads, can be mastered reliably using SIOV-AUTO varistors.

3.8.3 Fine protection

Electronic components are often far apart, so EMC cannot be implemented with a central suppressor module alone. Instead one has to provide extra fine protection directly on the individual modules. Here energy absorption of a few Joules to some tens of Joules is adequate, meaning that lower rated and thus smaller components can be chosen, like the SMD series SIOV-CU/CN or SHCVs. Figure 40 illustrates an EMC concept with varistors.

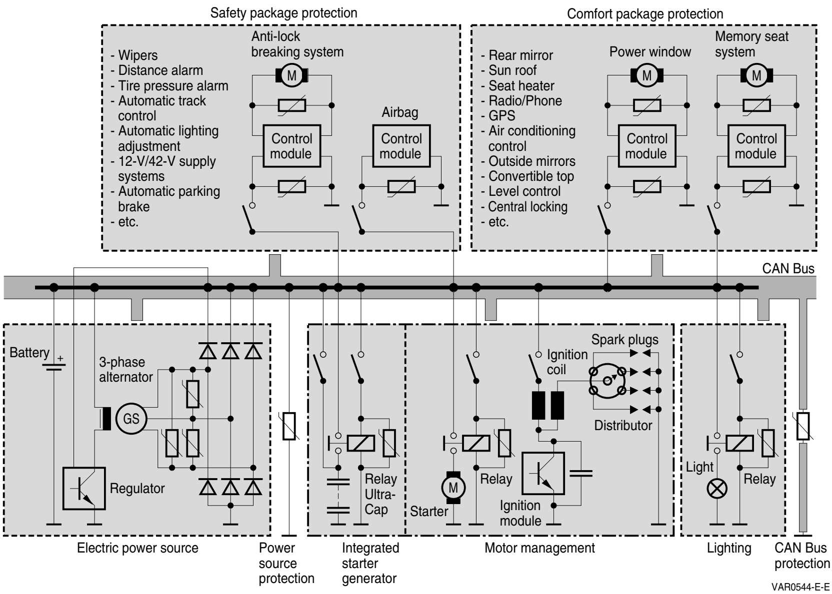


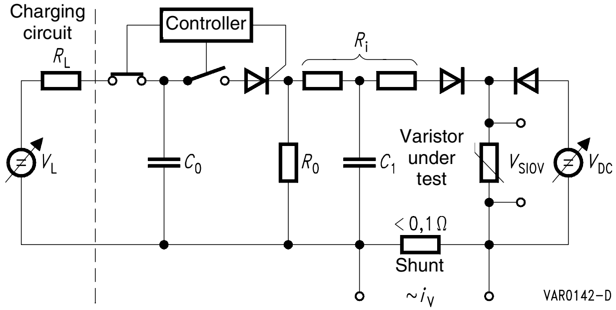
Figure 40 Automotive electrical system, complete EMC concept with varistors

3.8.4 Tests

Maintenance of EMC requirements can be checked with conventional test generators. Figures 41a and b show block diagrams for load dump tests with operating voltage applied. The electrical performance associated with a load dump of 100 J is illustrated in figures 42a to c.

Note:

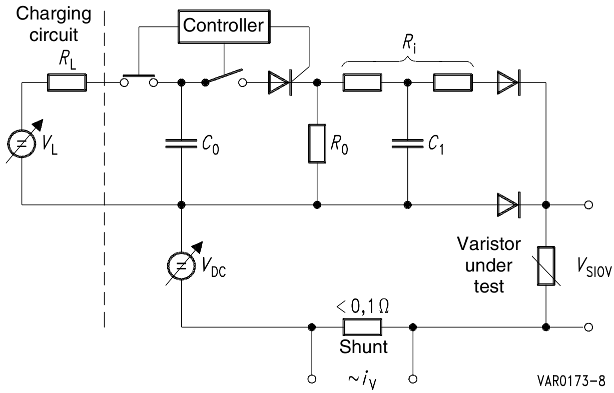
Circuit 41b produces the test pulse 5 according to ISO 7637 (DIN 40 839); the 10 % time constant t_d can be set independently of the battery voltage. Note that the maximum discharge current is not limited by the source V_{DC}.



Typical values

C_0	20 … 35 mF
R_0	4 … 10 Ω
C_1	0 … 10 µF
R_i	0,5 … 4 Ω
V_L	0 … 200 V
V_{DC}	12 … 28 V
t_d	100 … 800 ms
v_{SIOV}	Protection level of varistor
i_v	Current through varistor

Figure 41a Principle of load dump generator with battery connected in parallel

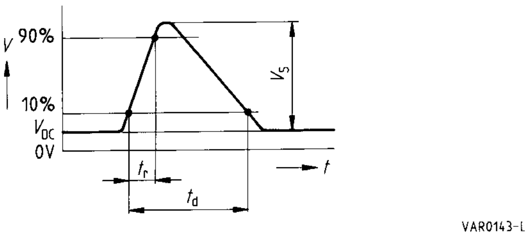


Typical values

C_0	4,7 … 47 mF
R_0	4 … 5 Ω
C_1	47 … 470 µF
R_i	0,5 … 5 Ω
V_L	0 … 200 V
V_{DC}	12 … 28 V
t_d	40 … 500 ms
v_{SIOV}	Protection level of varistor
i_v	Current through varistor

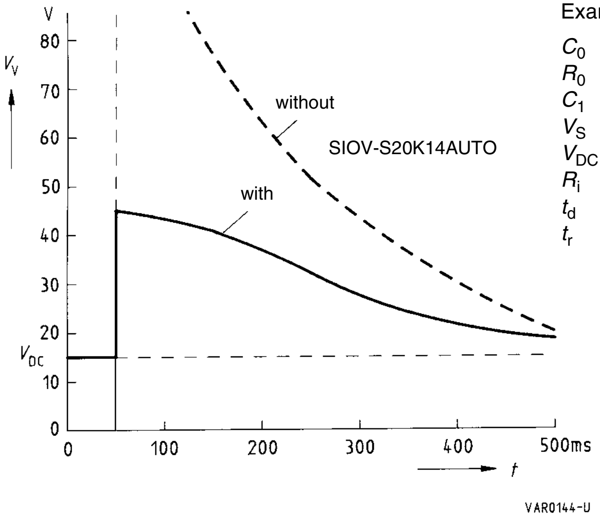
Figure 41b Principle of load dump generator with battery connected in series

42a



Test pulse 5
acc. ISO 7637
(DIN 40 839)

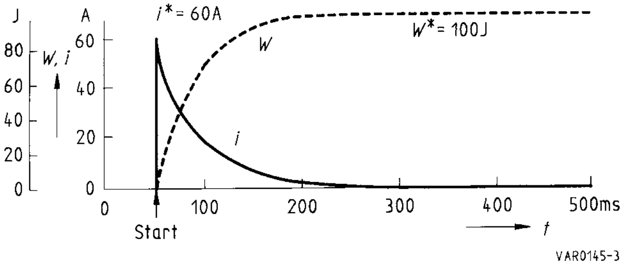
42b



Example:

C_0	37,6 mF
R_0	4,6 Ω
C_1	47 µF
V_S	146 V
V_{DC}	14 V
R_i	2 Ω
t_d	400 ms
t_r	0,1 ms

42c



Figures 42a – c Voltage (b), current and energy absorption (c) on SIOV-S20K14AUTO with test pulse 5 (a), load dump generator as in figure 41b

3.8.5 Load dump simulation using PSpice software, e. g. PSpice simulation of the load dump energy

The time region of the varistor current derating graphs is only shown for up to 10 ms, whereas the load dump duration can be as long as 400 ms.

To cover also the load dump condition, the automotive product tables show supplementary maximum energy values for load dump absorption (10 ×).

In accordance with ISO 7637, the load dump pulse 5 is specified by the parameters

- Charge voltage (test level) V_s
- Internal resistance R_i
- Rise time t_r
- Duration t_d

(see figure 42a).

The easiest way is to perform a software-simulation (using e. g. PSpice) to determine the amount of energy dissipation by the varistor, which portion of the energy of this pulse the varistor absorbs. As stated in equation 10, the value calculated by this method must be lower than the value specified in the product tables.

ISO 7637 requires that at least one load dump absorption must be tolerated.

In other specifications repeated load dumps up to 10 times are permissible. In coincidence with such regulations the automotive industry specifies load dump values for 10 repetitions for their applications.

EPCOS offers to perform load dump simulations according to customers' specifications upon special request.

For such cases, we require information concerning:

V_s, R_i, t_r, t_d and the number of repetitions desired.

3.8.6 42-V vehicle power supply

For the 42-V vehicle on-board power supply network, which is currently in the introductory stage, EPCOS is offering the varistor type series SIOV-S..V42AUTO. For details, please refer to the automotive product tables; ref. page 193.

Remark: PSpice is a registered trade mark of MicroSim Cooperation.
For a. m. software we are offering varistor simulation models.

3.8.7 RFI suppression

The capacitance of varistors alone (some nF) is not enough for RFI suppression. Therefore EPCOS has developed the high-capacitive varistors SHCV (**S**uper **HiC**ap **V**aristors) that offer transient protection and RFI suppression in very compact form. These components are comprised of a multilayer varistor connected in parallel with a multilayer capacitor. SHCVs are especially suitable for handling RFI from small motors of windscreen wipers, power windows, memory seats, central locking, etc. Figure 43 shows an example of the suppression effect.

EPCOS has extended its product range to include capacitances of up to 4,7 µF.

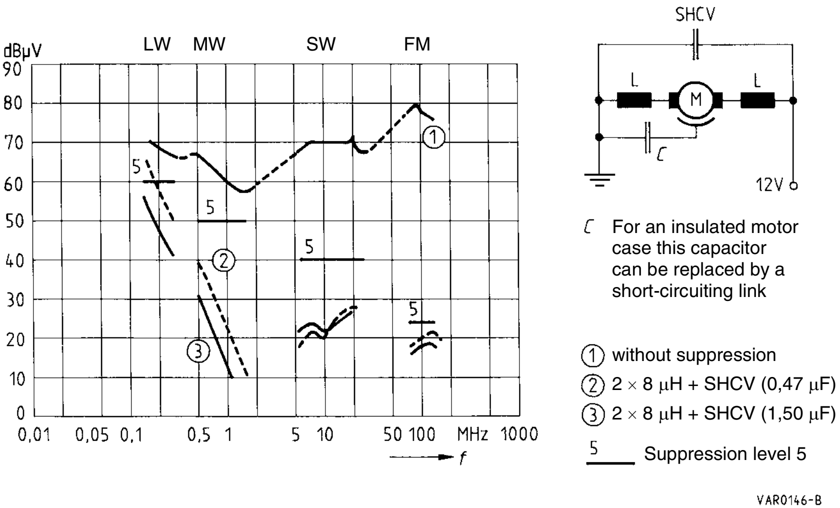


Figure 43 Example of RFI suppression in small motors with chokes and SHCVs (measured to VDE 0879, part 3)

3.9 Telecommunications

Electromagnetic interference on telecommunications, signal and control lines can be quite considerable as these lines tend to be long and exposed. So the requirements are correspondingly high when it comes to the electromagnetic compatibility of connected components or equipment.

3.9.1 Standard program

Disk-type SIOVs are used all over the world as reliable protection components in communications terminal devices (e.g. telephones) and in switching exchange systems (e.g. line cards).

Depending on the test severity of the specifications, type series SIOV-S07, -S10, -S14, -S20, SIOV-CT/CN1812 and SIOV-CU4032 with the voltage levels K60 to K230 are used in such applications.

The easiest method of selecting a varistor is to use PSpice simulation to select a varistor for given requirements. In 3.10.2, the calculation shows if SIOV-S10K95 is acceptable.

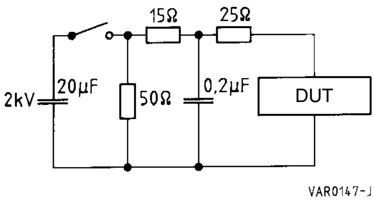
3.9.2 Telecom varistors

According to the directives of the Central Telecommunications Engineering Bureau (Fernmeldetechnisches Zentralamt FTZ) of Germany's telecommunications administration the immunity of telecomms equipment must be tested with the increased surge voltage of 2 kV (ITU-T only specifies 1,0 and 1,5 kV). The wave shape is 10/700 µs according to ITU-T and IEC 61000-4-5. Figure 44 shows the simplified test circuit diagram.

To meet these more severe test conditions, EPCOS has developed special "Telecom" varistors which can absorb the energy of such 2 kV surge loads as specified in the test regulations (10 times; 5 times for each polarity).

As shown in the product tables, these Telecom versions are available in the styles

- Disk, radial SIOV-S07 (TELE)
- SMD molded SIOV-CU4032 (TELE)
- SMD multilayer SIOV-CT/CN1812 (TELE)



DUT Device under test
e.g. telephone terminal device

Figure 44 Circuit for generating 10/700 µs test pulse to ITU-T and IEC 61000-4-5

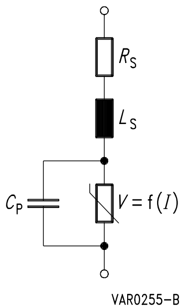
3.10 EPCOS PSpice simulation model

3.10.1 Varistor model

The development of a SIOV model for the “PSpice Design Center” circuit simulation program allows varistors to be integrated into the computer-assisted development of modern electronic circuitry.

In the PSpice modelling concept, the varistor is represented by its *V*/*I* characteristic curve, a parallel capacitance and a series inductance.

The structure of this equivalent circuit is shown in figure 45.



$V = f(I)$	*V*/*I* characteristic
C_p	Varistor capacitance
L_s	Series inductance
$R_S = 100\ \mu\Omega$	Series resistance

Figure 45 Varistor model, basic structure

In the model, the *V*/*I* characteristic curve is implemented by a controlled voltage source $V = f(I)$. An additional series resistance $R_s = 100\ \mu\Omega$ has been inserted in order to prevent the unpermissible state which would occur if ideal sources were to be connected in parallel or the varistor model were to be connected directly to a source.

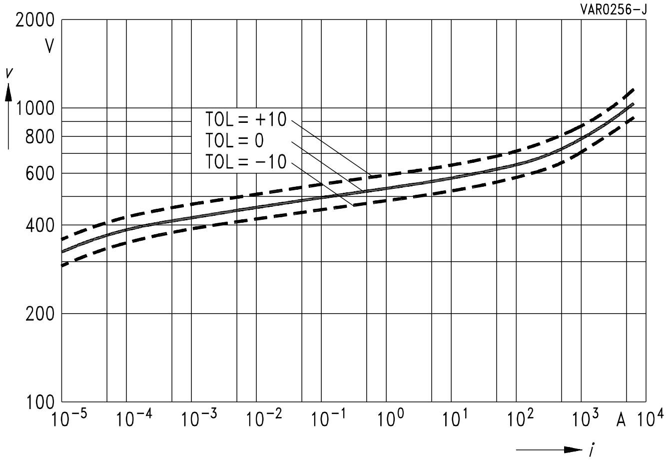
The following approximation is used for the mathematical description:

$$\log V = b1 + b2 \cdot \log(I) + b3 \cdot e^{-\log(I)} + b4 \cdot e^{\log(I)} \qquad I > 0 \qquad \text{(equ. 21)}$$

This means that the characteristic curve for any specific varistor can be described by the parameters b1 … b4. Figure 46 shows the typical *V*/*I* characteristic curve for the varistor SIOV-S20K275 and the corresponding parameters b1 … b4.

The tolerance bandwidth of the *V*/*I* characteristic curve can be shifted (cf. figure 7) in order to include cases of

- upper tolerance bandwidth limit:
  highest possible protection level for a given surge current, and
- lower tolerance bandwidth limit:
  highest possible (leakage) current for a given voltage.



b1 = 2.7233755
b2 = 0.0258453
b3 = 0.0005746
b4 = 0.0046033

Figure 46 *V/I* characteristic curve of SIOV-S20K275 with tolerance band

In the model, the capacitance values stated in the product tables are used. The dependence of the capacitance on the applied voltage and frequency is extremely low and can be neglected here.

It is not permissible to neglect the inductance of the varistor in applications with steep pulse leading edges. For this reason, it is represented by a series inductance and essentially is determined by the lead inductance. As opposed to this, the internal inductance of the metal oxide varistor may be neglected. The inductance values in the model library are chosen for typical applications, e.g. approx. 13 nH for the S20K275. If longer leads are used, insertion of additional inductances must be considered, if necessary. In the case of disk varistors, the inductance of the leads is approx. 1 nH/mm.

The PSpice simulation models can be downloaded from the Internet (www.epcos.com/tools).

Limits of the varistor model

For mathematical reasons, the *V/I* characteristic curves are extended in both directions beyond the current range (10 µA up to I_{max}) specified in this data book, and cannot be limited by the program procedure. The validity of the model breaks down if the specified current range is exceeded. For this reason, it is imperative that the user takes consideration of these limits when specifying the task; the upper limit depends on the type of varistor. Values of < 10 µA may lead to incorrect results, but do not endanger the component. In varistor applications, it is only necessary to know the exact values for the leakage current in the < 10 µA range in exceptional cases. As opposed to this, values exceeding the type-specific surge current I_{max}, may lead not only to incorrect results in actual practice but also to destruction of the component. Apart from this, the varistor model does not check adherence to other limit values such as maximum continuous power dissipation or surge current deratings. In addition to carrying out simulation procedures, the adherence to such limits must always be ensured, observing the relevant spec given in the data book.

In critical applications, the simulation result should be verified by a test circuit.

The model does not take into account the low temperature coefficient of the varistors (equ. 7).

3.10.2 Example for the selection with PSpice

In this example, the aim is to test whether selecting a standard varistor SIOV-S10K95 would meet the test conditions specified by the German Telecommunications Administration:

Figure 44 shows the test circuit with a 2 kV charge voltage, figure 47 shows the corresponding model used in PSpice.

In order to achieve an open-circuit voltage of 2 kV, the charging capacitor must be charged to 2,05 kV. In order to prevent an undefined floating of R_{m2}, an additional resistor R_1 = 10 MΩ is inserted at the output end.

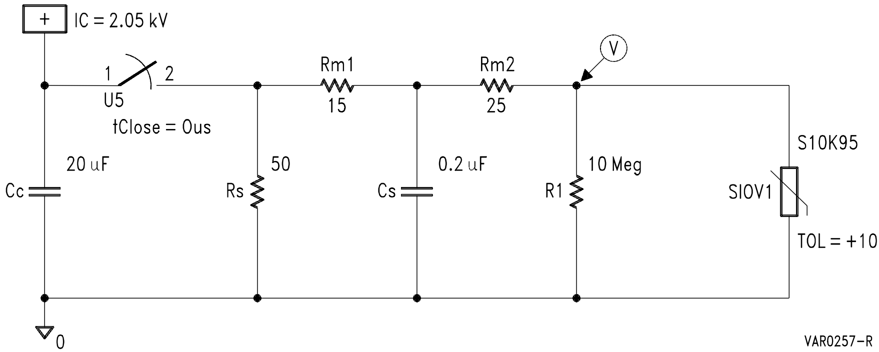


Figure 47 Simulation of the test pulse 10/700 µs applied to the device under test S10K95

For the varistor, the upper characteristic curve tolerance (TOL = +10) limit is used to simulate the worst case i.e. highest possible protection level. It is not considered necessary to model the device to be protected in this diagram, since, in relation to the varistor, this is generally of higher resistance for pulse loads.

Figure 48 shows the curve of the open-circuit voltage (varistor disconnected) and the maximum protection level (with varistor).

Surge current

Figure 49 shows the voltage and current curves, with the $\int i^* \, dt$ included in the drawing.

A maximum current of 44 A can be deduced from the curves.

Then, according to equation 14:

$$t^*_r = \frac{\int i^* \, dt}{\hat{i}^*} = \frac{17 \text{ mAs}}{44 \text{ A}} \approx 386 \ \mu s$$

According to figure 50, the resulting maximum surge current for 10 loads is i_{max} = 48 A > $\hat{i}^*$ = 44 A. The selection criterion of equ. 9 is fulfilled.

Energy absorption

PSpice displays the energy absorption directly as $W^* = \int v^* i^* dt = 4{,}2$ J.

The resulting permissible time interval between two pulses according to equ. 20 is:

$$T_{min} = \frac{W^*}{P_{max}} = \frac{4{,}2\ \text{J}}{0{,}4\ \text{W}} = 10{,}5\ \text{s}$$

This means that the requirement of a minimum time interval between pulses of 60 s or more is fulfilled.

Highest possible protection level

Figure 48 shows the highest possible protection level to be 260 V. Thus it is possible to reduce the “overvoltage” of 2 kV to 13 % of its value.

Note:
The specification stated above can also be met using the specially developed Telecom varistors (cf. section 3.9.2).

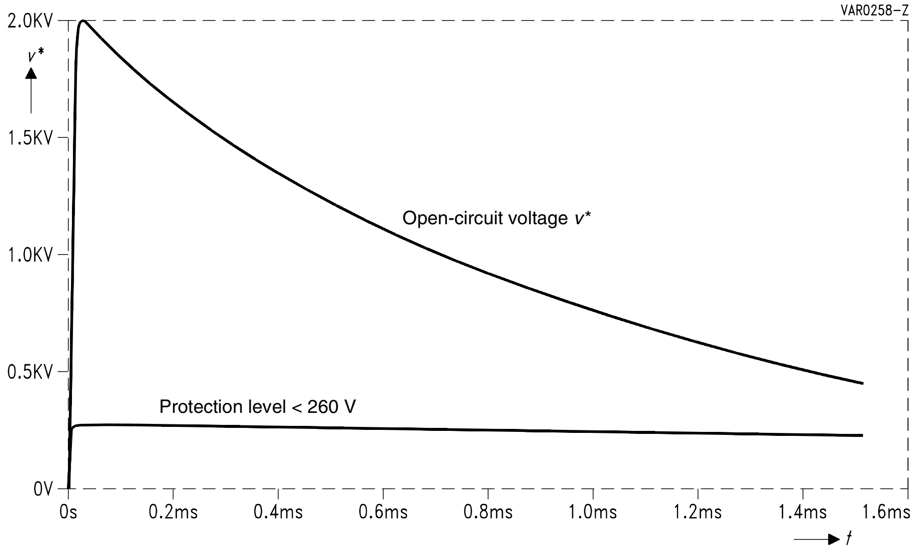


Figure 48 Open-circuit voltage (varistor disconnected) and maximum protection level (with varistor) achieved by the SIOV-S10K95 varistor

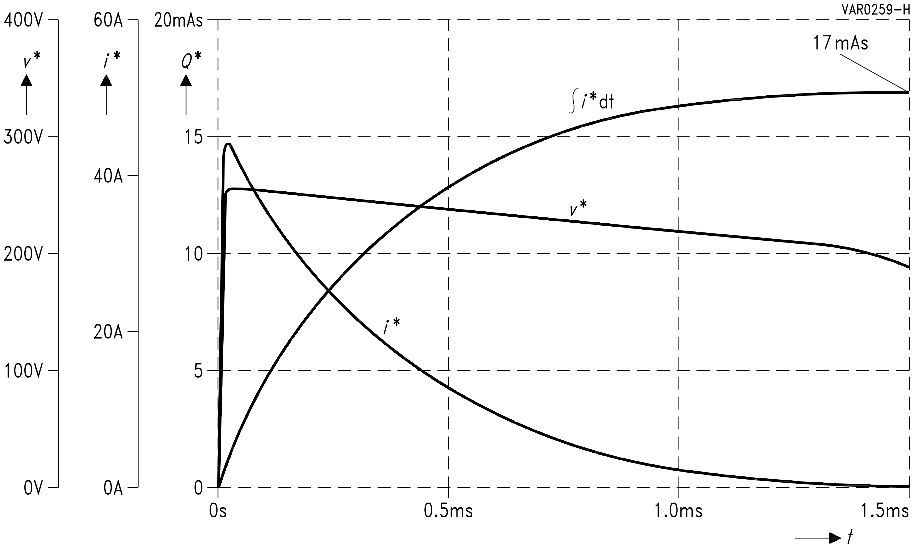


Figure 49 PSpice simulation: voltage, current and $\int i^* dt$ curves for the S10K95

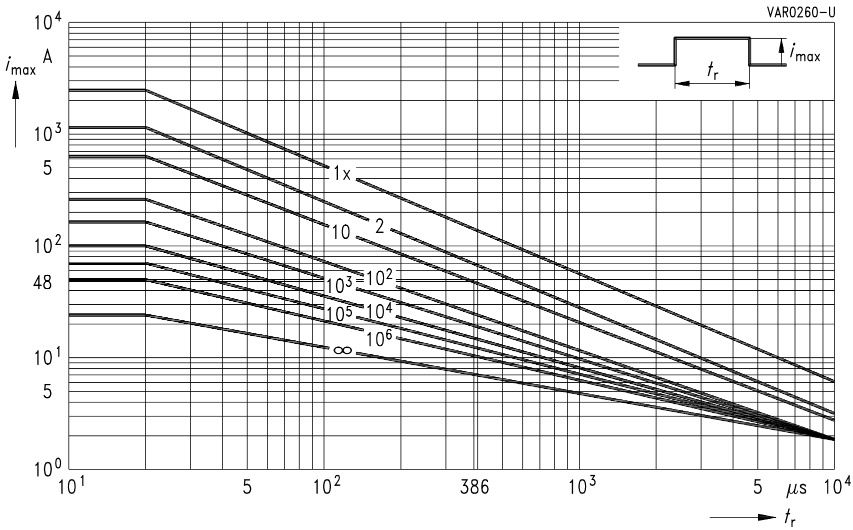


Figure 50 A maximum surge current i_{max} = 48 A (10 times) can be deduced for t^*_r = 386 µs from the derating curves for S10K50 … 320

3.11 Combined circuits

3.11.1 Stepped protection

If transient problems cannot be resolved with a single component like a varistor, it is always possible to combine different components and utilize their respective advantages. As an example, figure 51 illustrates the principle of stepped protection of a telemetry line with a gas-filled surge arrester [1], a varistor and a suppressor diode*):

The voltage of 10 kV is limited in three stages

- "coarse" surge arrester
- "standard" varistor
- "fine" suppressor diode, zener diode or filter [2]

to less than 50 V. The series inductors or resistors are necessary to decouple the voltage stages.

Note:
According to the specifications in [1] gas-filled surge arresters may not be used on low-impedance supply lines.

3.11.2 Protective modules

Application-specific circuits for stepped protection assembled as modules, some incorporating overload protection and remote signaling, are available on the market.

Figures 52a and b show some practical examples.

[1] Shortform catalog "Gas-Filled Surge Arresters", ordering no. EPC: 48001-7400
[2] Data book "EMC Filters", ordering no. EPC: 24004-7600
*) Not in the EPCOS product range

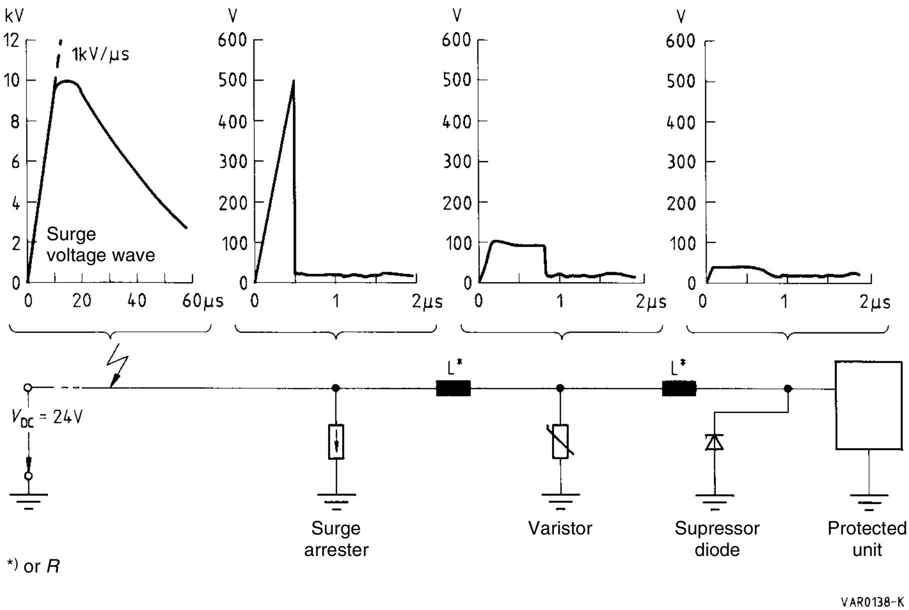
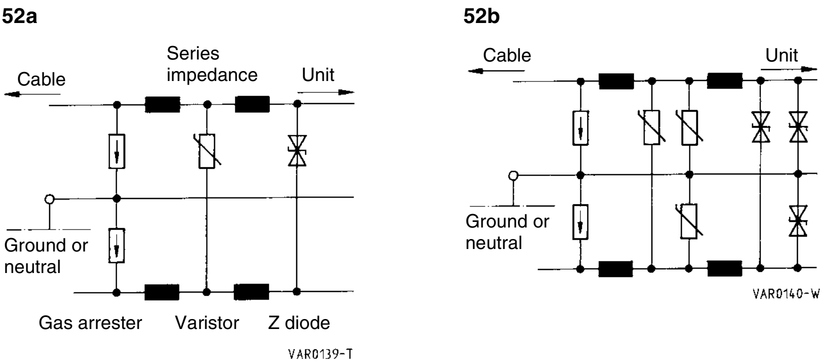


Figure 51 Principle of stepped protection with surge arrester, varistor and suppressor diode



Figures 52a and b Examples of transient protective modules

a) Circuit with coarse protection plus fine transverse voltage protection
b) Circuit with coarse protection plus fine longitudinal voltage and transverse voltage protection

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