

Attracting Tomorrow



Ceramic capacitor technology

CeraLink® opens new dimensions
in power electronics

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CeraLink in a shot - optimized for conditions under operation in power electronics

Use CeraLink when

- Space requirement is tight
- Temperature is demanding (+150 °C)
- High current rating is vital
- Requirements for capacitance density are tough
- High switching frequencies are applied (SiC, GaN)

Main function in HV application

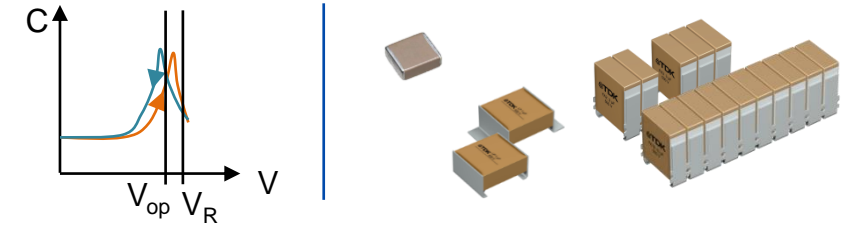
- Snubber capacitor
- Filter capacitor
- Flying capacitor
- DC-Link capacitor

CeraLink technology supports

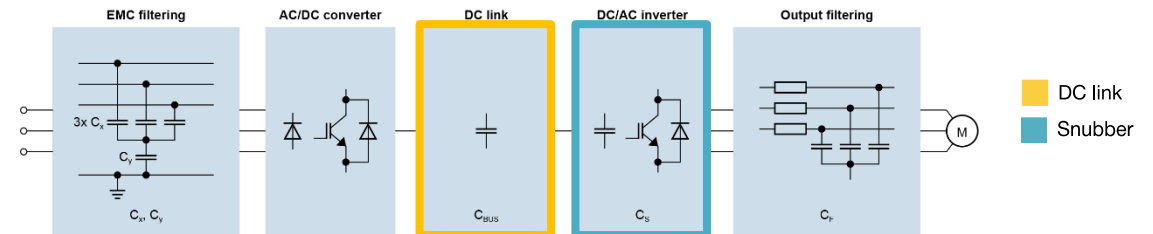
- Increasing capacitance with DC bias and best in class capacitance density at operating point ($V_{op} + T_{op}$)
- High current capability due to low losses at high frequencies (up to several MHz) and high temperatures (up to +150 °C)
- No limitation of dV/dt
- Good self-regulating properties
- Qualification based on AEC-Q200 rev. D



Full performance potential



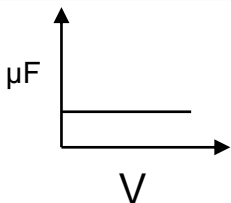
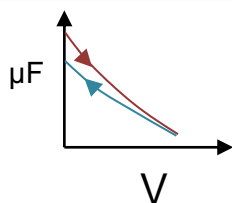
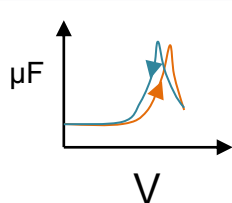
Principle circuit diagram of function of capacitors in e.g. motor drives

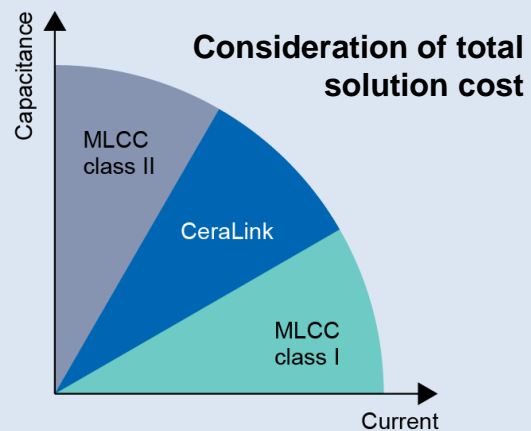


Measurement condition	Film capacitor	MLCC class II	CeraLink
Typical capacitance density @ DC link voltage, 20 V_{RMS} , 25 °C	0.7 $\mu F/cm^3$	2.5 $\mu F/cm^3$	4.9 $\mu F/cm^3$
Typical current rating per capacitance @ 100 kHz, 105 °C	< 1 A/ μF	< 4.5 A/ μF	11 A/ μF

CeraLink's special behaviour ①

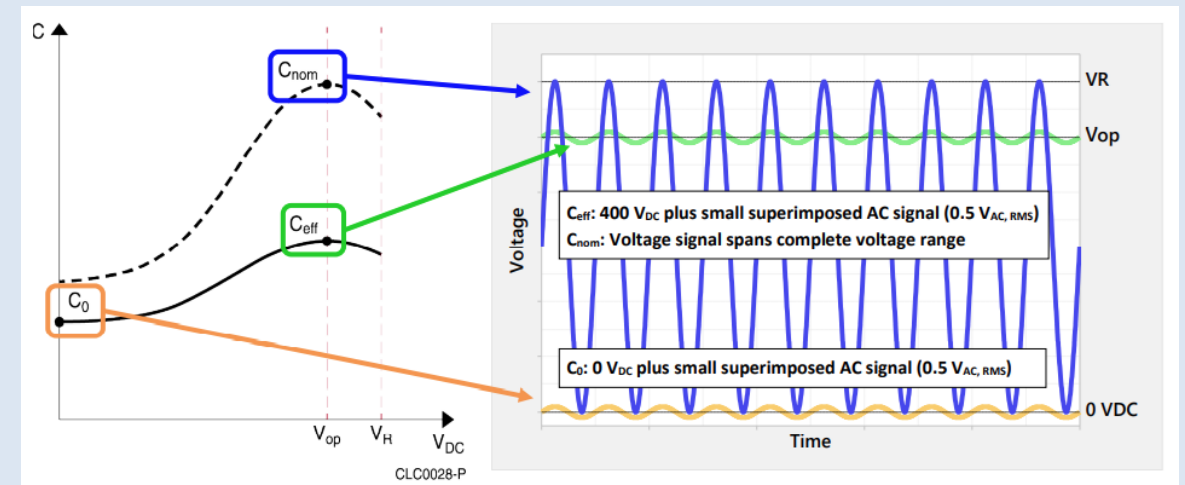
Some differences to MLCC

Linear	Ferroelectric	Antiferroelectric
MLCC class I	MLCC class II	CeraLink
		



Feature: Positive bias behaviour

- Increasing capacitance with DC bias between 0 V and V_{op}
- Best in class capacitance density at operating point (V_{op} & T_{op})



More to this in the CeraLink
Technical Guide



CeraLink's special behaviour ②

At high temperature

- Operating temperature up to +150 °C
- Low losses at high temperature
- Low leakage current
- No thermal runaway
- Generally low self-heating AND self-heating supports CeraLink to come to temperature for good performance

At high frequency

- Optimal frequency in the range of 100 kHz to 1 MHz
- Minimal ESR due to low-loss copper electrodes and HF-suited backend
- Typ. ESR @ 25 °C, 1 MHz*: 3 ... 45 mΩ
- Typ. ESL*: 2 ... 4 nH
- No limitation of dV/dt
- Temperature decrease with rising frequency

Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions

Measurement condition	MKP film capacitor	MLCC class II (BTO)	CeraLink
Typical capacitance density @ DC link voltage, 20 V _{RMS} , 25 °C	0.7 µF/cm ³	2.5 µF/cm ³	4.9 µF/cm³
Typical current rating per capacitance @ 100 kHz, 105 °C	< 1 A/µF	< 4.5 A/µF	11 A/µF

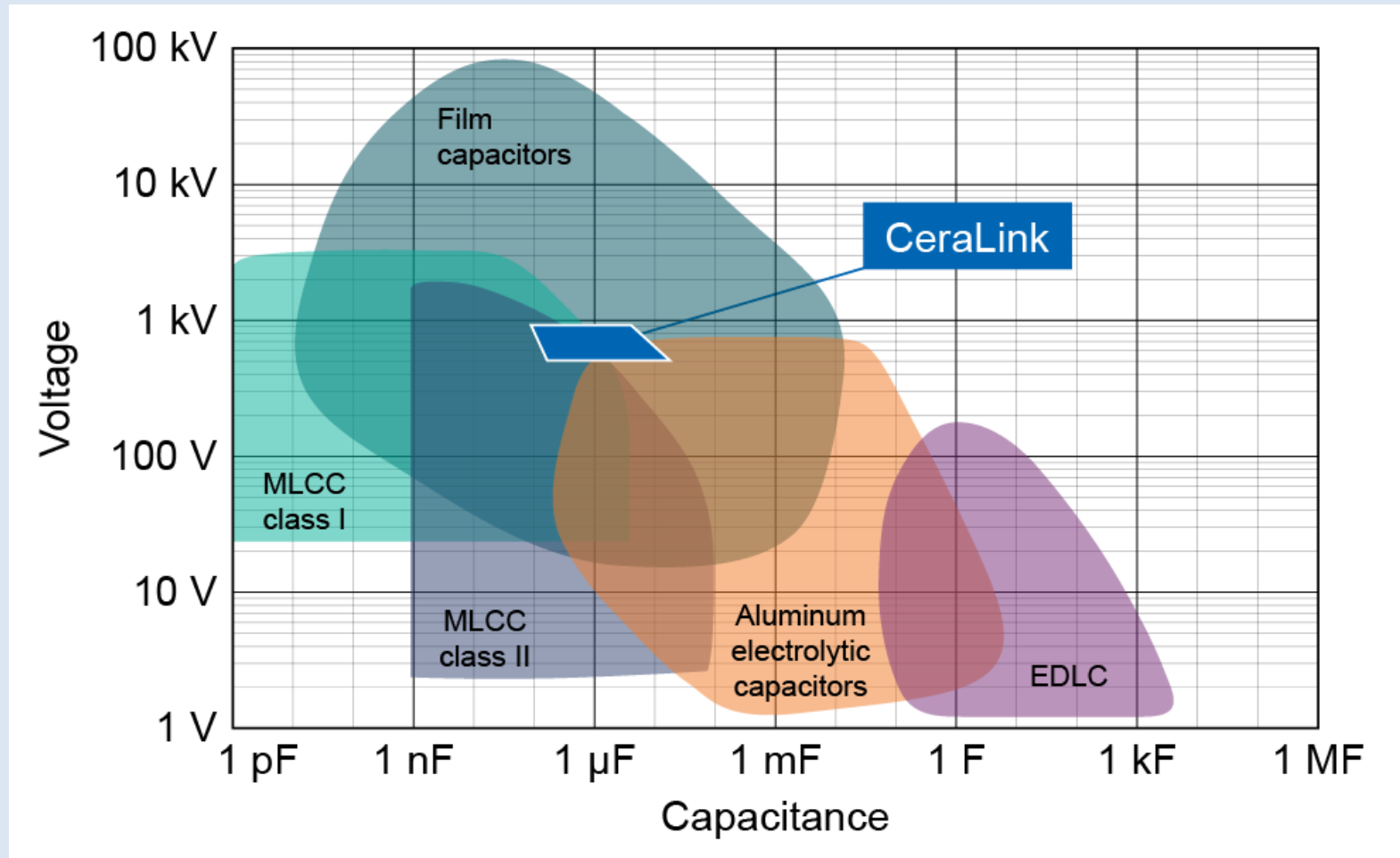
*varies with series and voltage class

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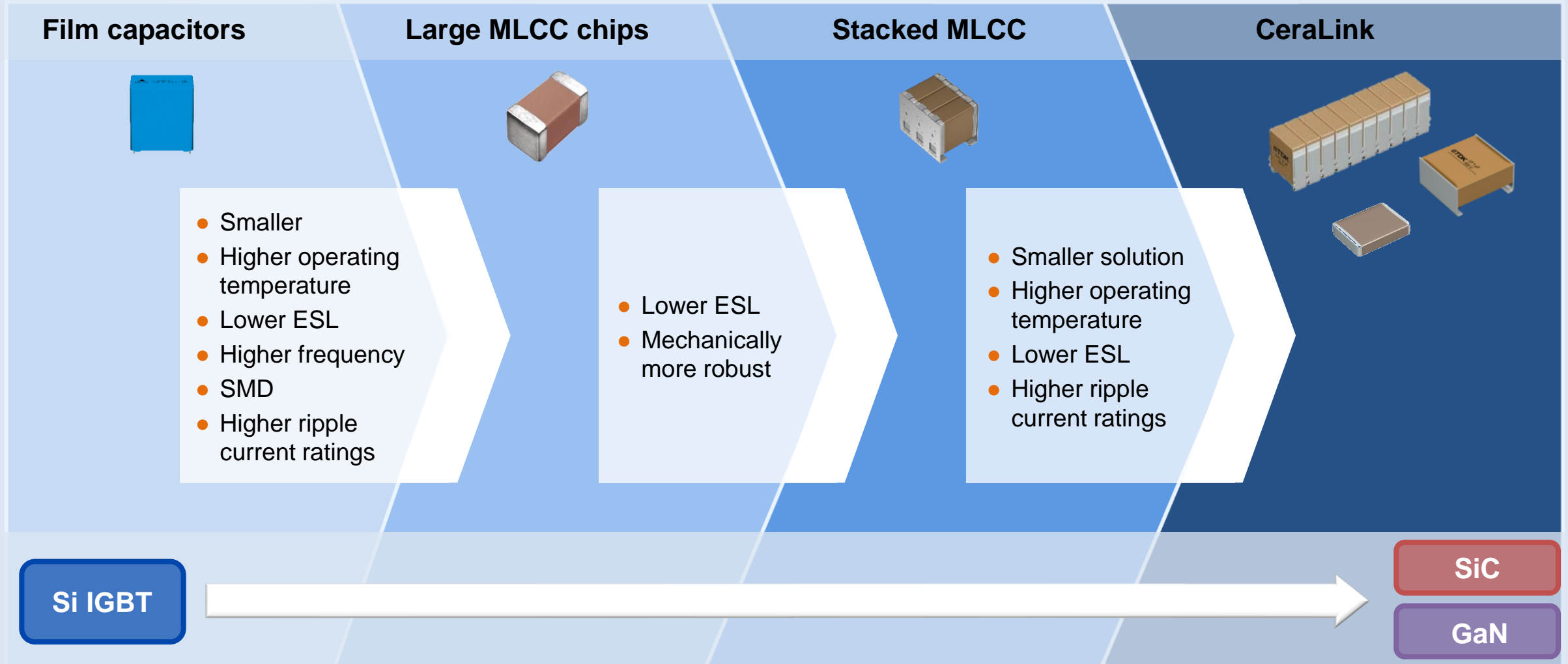


Technology Insights

Capacitor technology landscape



Technology guideline



Positioning CeraLink in capacitor landscape

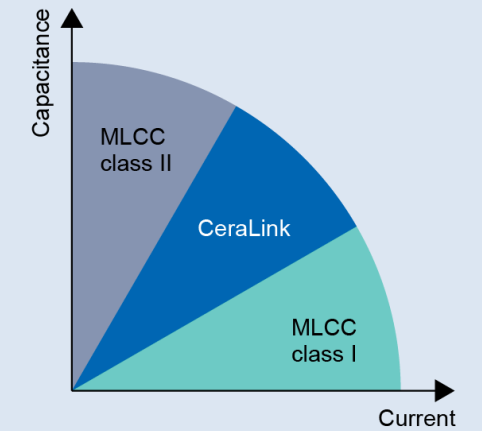
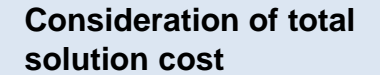


General

Capacitance at voltage	Film capacitor	MLCC class II	CeraLink
Nom. / rated capacitance	100%	100%	100%
No bias voltage 0.5 V _{RMS}	100%	100%	35%
DC link voltage 0.5 V _{RMS}	100%	35%	60%
DC link voltage 20 V _{RMS}	100%	35%	100%

Ceramic landscape

Special requirements	MLCC class I	MLCC class II	CeraLink
Resonance, stable C	✓	✗	✗
T >125 °C	✓	X8R / custom	✓
V >630 V	✓	Limited offer	✓
AC	✓	✓	✗
Current			

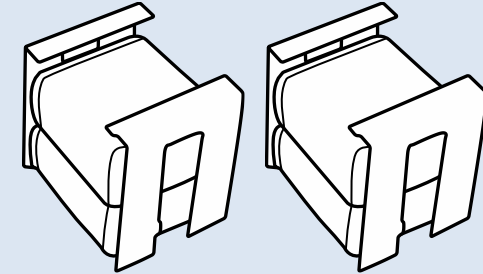


CeraLink LP versus MLCC class II

Capacitance
@ 400 V + 20 V ripple



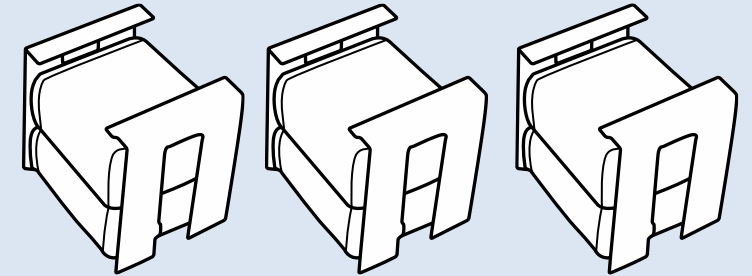
Similar like



Ripple current
@ 100 kHz & 85 °C



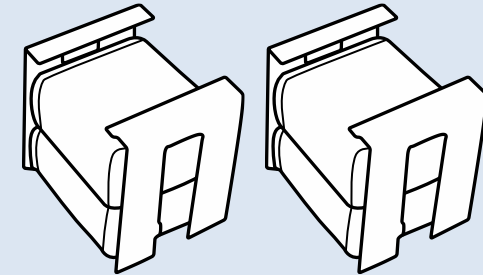
Similar like



Added value of
CeraLink LP series



- Less PCB space
- Higher temperature
- Low ESL

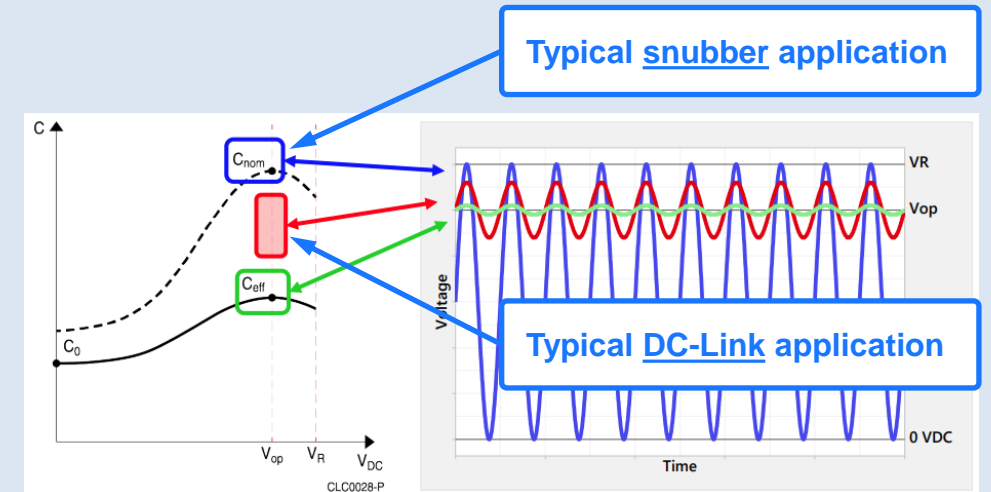
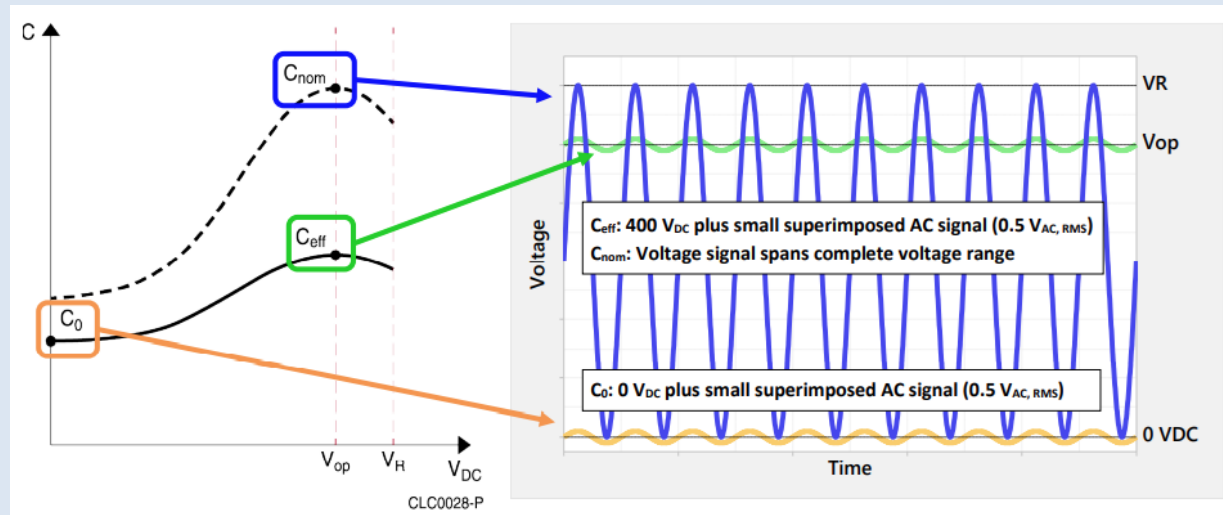


Stacked MLCC based on case size 2220

CeraLink's special behaviour... (1)

... positive bias behaviour

CeraLink features a non-linear capacitance behavior, i.e. the capacitance strongly depends on external parameters such as the applied DC bias voltage or the temperature. It is important to note that CeraLink is designed to have its capacitance maximum under operating conditions, i.e. under a DC bias (constant operating voltage) and with a superimposed ripple amplitude.



More to this in the CeraLink
Technical Guide

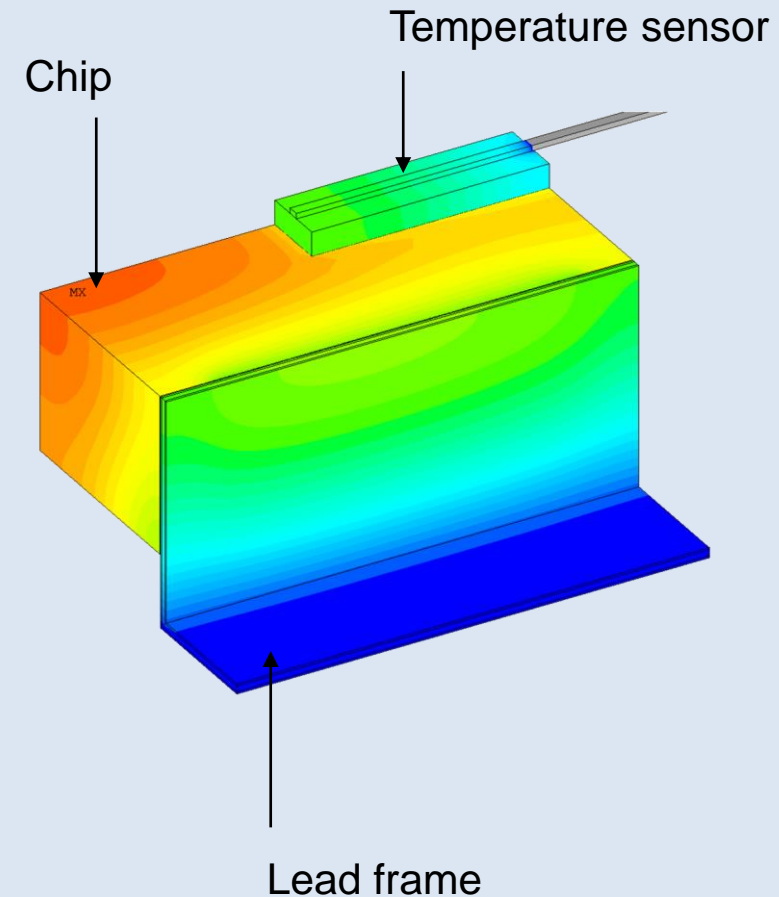


CeraLink's special behaviour... (2)

... at high temperatures

- Operating temperature up to +150 °C
- Low ESR
- Low leakage current
- No thermal runaway
- Superb heat transport capabilities to PCB due to copper-invar-copper (CIC) lead frames*
- High ripple currents of up to 11 A/μF
- Generally low self-heating AND self-heating supports CeraLink to come to temperature for good performance

*used for CeraLink® LP, FA and SP series



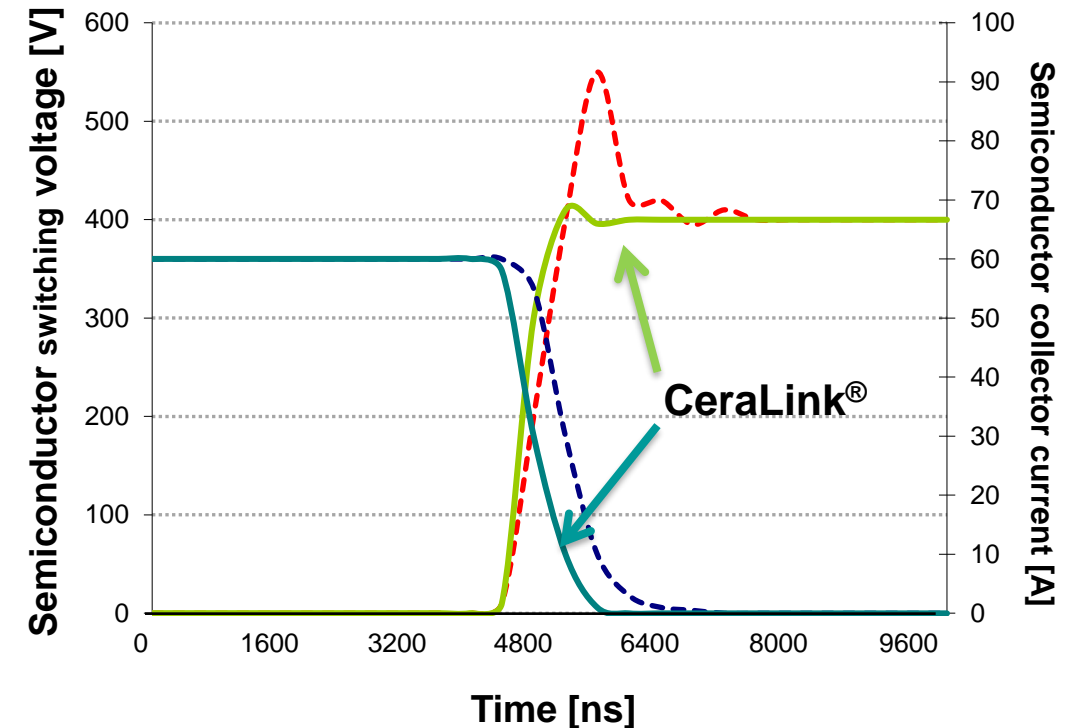
CeraLink's special behaviour... (3)

... at high frequencies

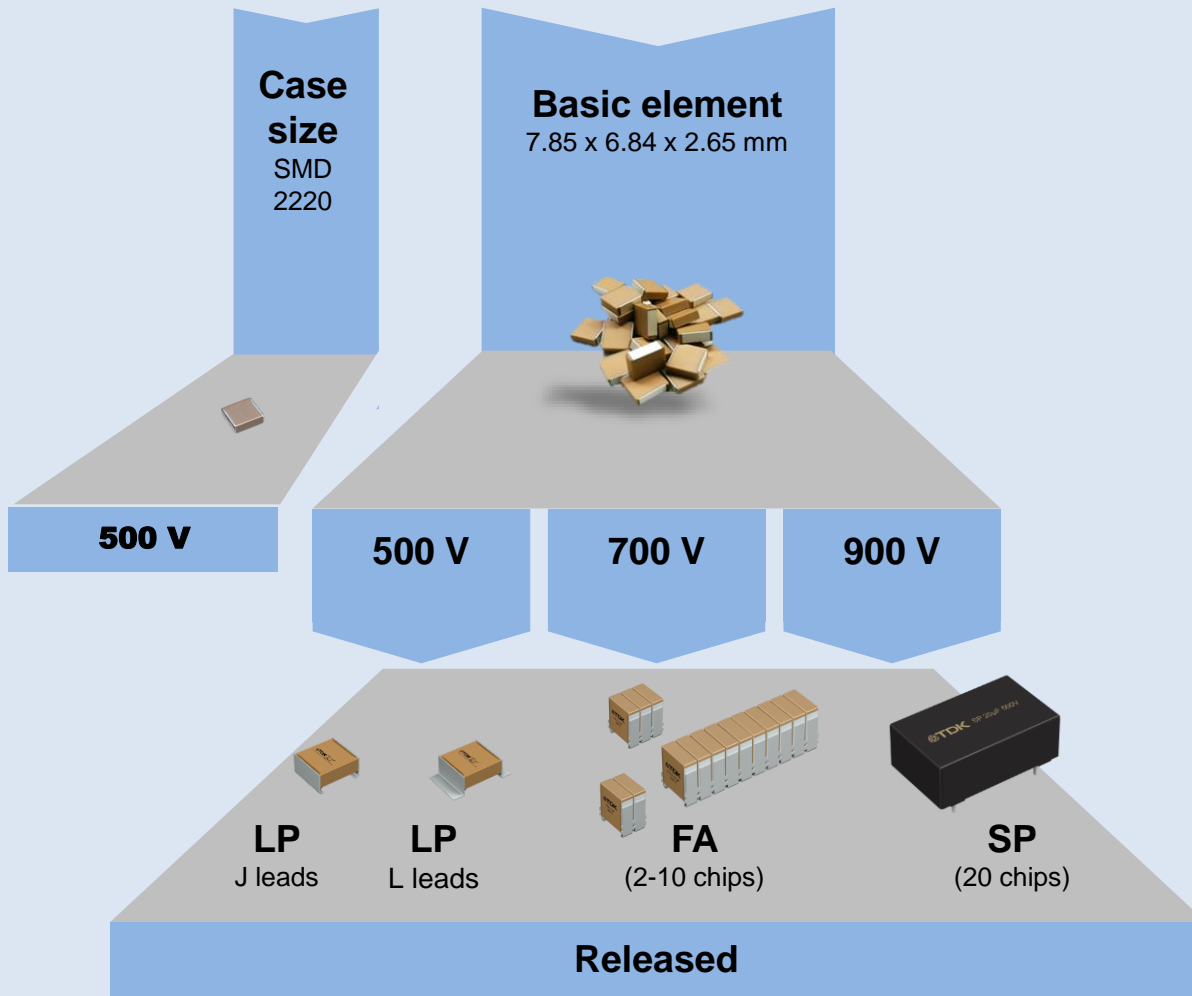
- Perfect for frequencies up to 1 MHz
 - No limitation of dV/dt
 - Minimal ESR at high temperatures due to low-loss copper electrodes and HF suited backend
 - Typ. ESL* 2 to 4 nH
- ➔ **Perfect as snubber or in filter applications**

*varies with series and voltage class

Semiconductor overshoot principle



CeraLink product portfolio



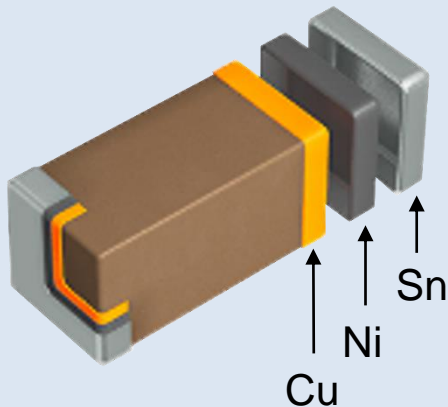
Series	Rated voltage		
	500 V	700 V	900 V
Low profile LP (L / J leads)	1 μ F	0.5 μ F	0.25 μ F
Flex assembly FA2 / FA3	2 / 3 μ F	1 / 1.5 μ F	0.5 / 0.75 μ F
Flex assembly FA10	10 μ F	5 μ F	2.5 μ F
Solder pin SP	20 μ F	10 μ F	5 μ F
2220 series SMD 2220 Standard + Soft Termination	0.25 μ F @ h: 1.4 mm		Coming soon

CeraLink SMD 2220 series

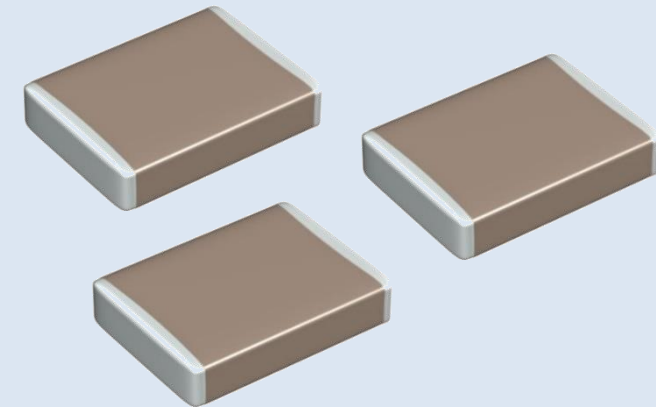
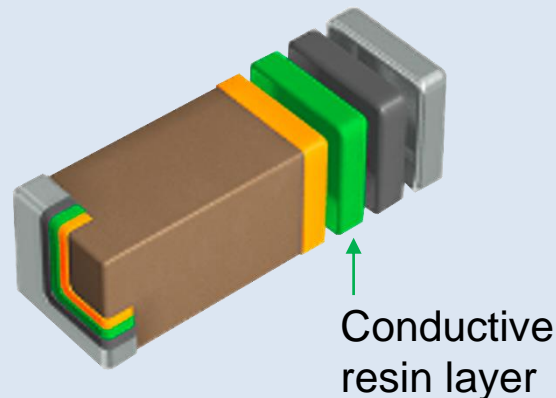
- Optimized for capacitance density (MLCC design)
- Termination
 - Standard: Cu cap with Ni/Sn galvanics
 - Soft electrode: additional conductive resin layer absorbing mechanical stress

- 500 V component with 1.4 mm height
 - $C_{\text{nom, typ}}$: 250 nF
 - I_{RMS} @100 kHz and 85 °C: 5 A

Regular terminal product



Soft termination



CeraLink product outlook

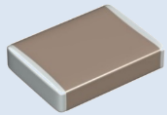
The chip size components

CeraLink SMD 2220 500 V

h: 1.4 mm

$C_{\text{nom, typ}}$: 250 nF

Released

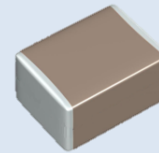


CeraLink SMD 2220

with maximum capacitance
due to higher height

500 V component

900 V component

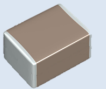


CeraLink SMD 1210 500 V

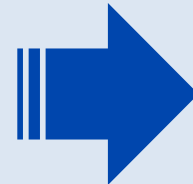
with maximum capacitance
due to higher height

500 V component

900 V component



All case sizes in both termination available:
Cu cap with Ni/Sn galvanics, soft electrode with
additional conductive resin



... other voltage classes

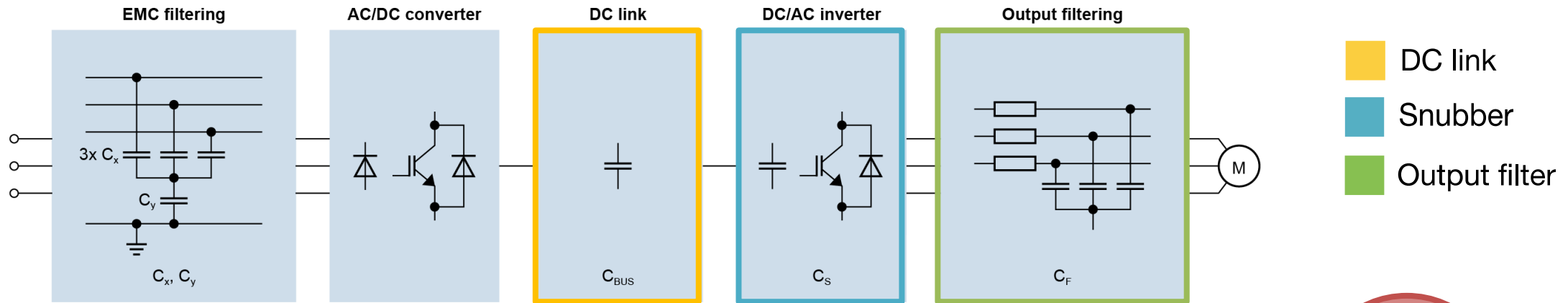
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Application Insights

CeraLink target applications

Principle circuit diagram of function of capacitors in e.g. motor drives

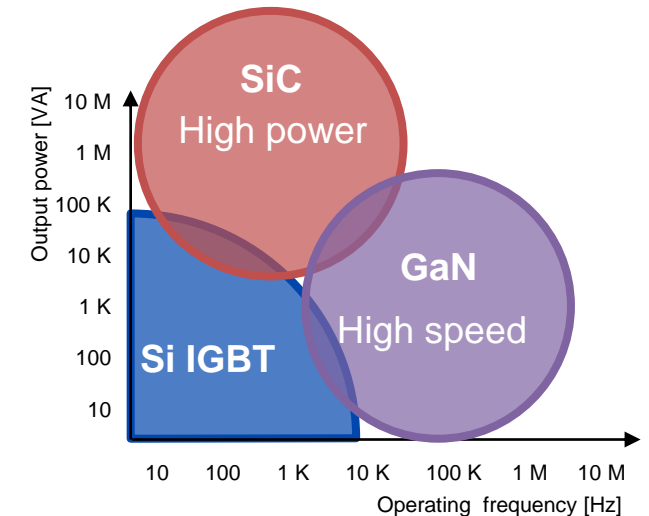


Main function

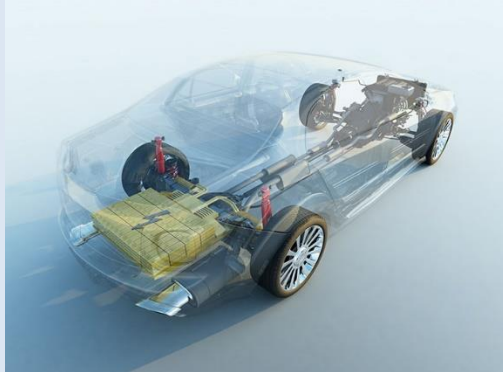
- Snubber capacitor
- Filter capacitor
- Flying capacitor
- DC-link capacitor

Scope

- High power density
- High efficiency
- High temperature



CeraLink[®]: Ideal for demanding applications (examples)



**High-voltage
applications in xEV**



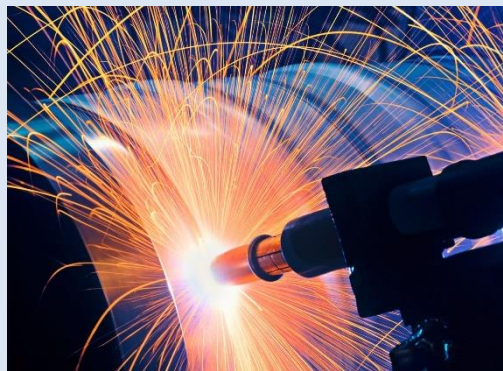
**Power supplies for
medical equipment**



**Test and
measurement**



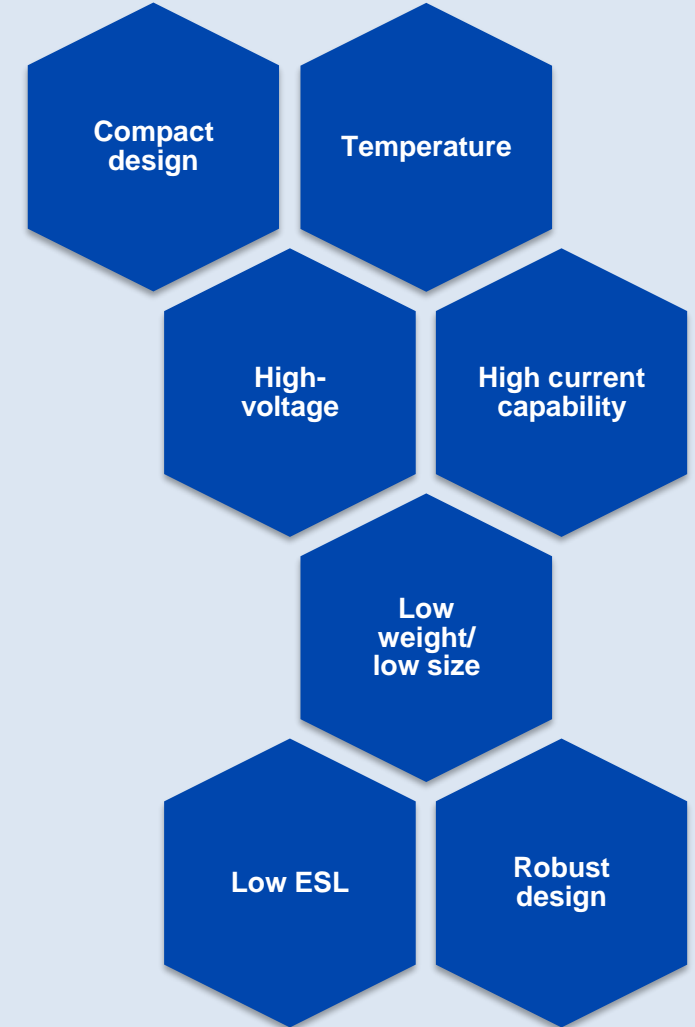
Drives





Welding



**Traction
(SiC)**

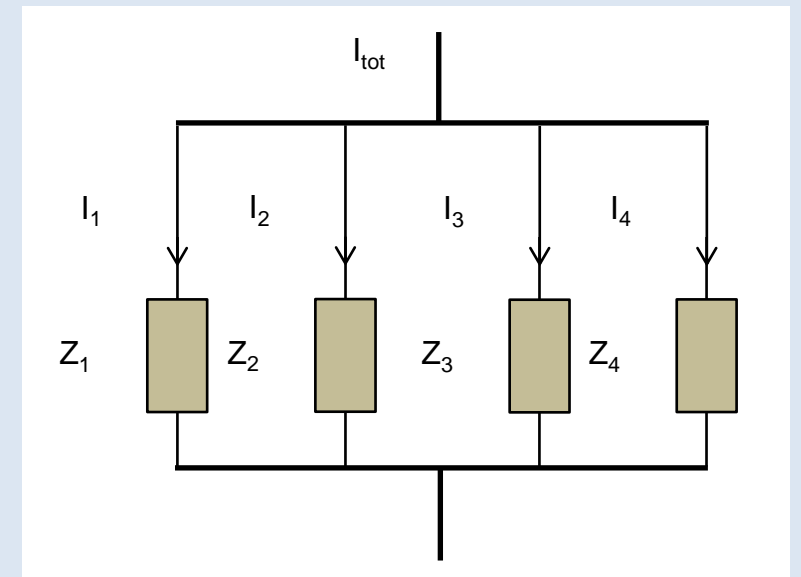


CeraLink as DC link

Series	Maximum voltage ratings			Features
	650 V	1000 V	1300 V	
Flex Assembly FA10 	10 μF / 500 V	5 μF / 700 V	2.5 μF / 900 V	The capacitance characteristic and low ESR of CeraLink avoid a thermal runaway
Solder Pin SP 	20 μF / 500 V	10 μF / 700 V	5 μF / 900 V	

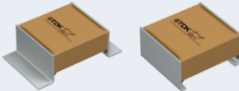


In parallel connection, higher temperature leads to:

- Lower capacitance
- Higher impedance
- Lowest current through the **hottest** capacitor → self-regulating properties



CeraLink as snubber

1 per half bridge - *mounted close to the semiconductor*

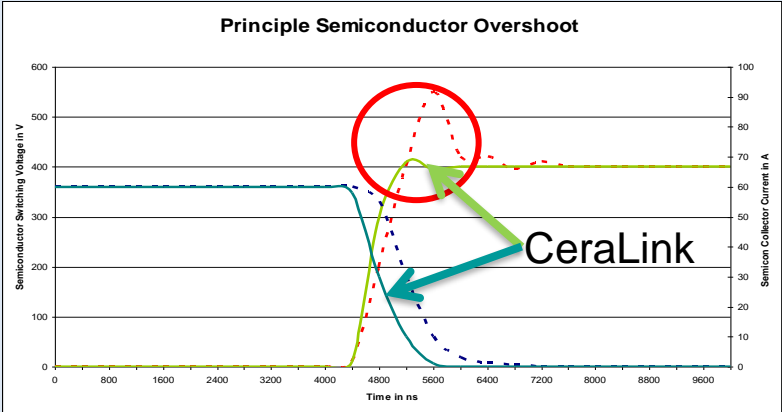
Series	Maximum voltage ratings			Features
	650 V	1000 V	1300 V	
Low Profile LP (L / J leads) 	1 µF / 500 V	0.5 µF / 700 V	0.25 µF / 900 V	<ul style="list-style-type: none">• Low ESL (typ. 3 nH)• Low losses at high frequencies and high temperatures (up to +150 °C)• No limitation of dV/dt
Flex Assembly FA2 / FA3 	2/3 µF / 500 V	1/1.5 µF / 700 V	0.5/0.75 µF / 900 V	
SMD SMD 2220 - New 	0.25 µF / 500 V @ h: 1.4 mm	Coming soon in new h: 1.9 mm		

Over-voltages or over-shoots occur when switching off a Semiconductor.

This will cause an overvoltage according the formula (see left)

The low inductance of the CeraLink enables a faster switching of the semiconductor resulting in lower switching losses, enabling a reduction of switching losses of up to **40%**!

$$V = -L \cdot \frac{di}{dt}$$



CeraLink: Ideal for demanding applications

Key facts

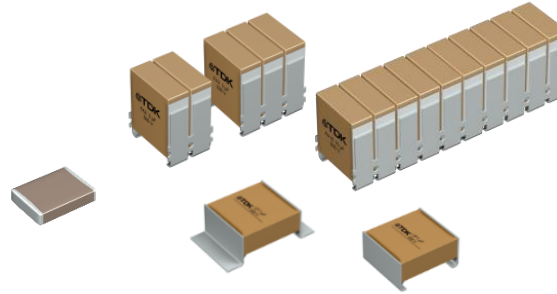
Target applications

Automotive

- OBC
- DC/DC
- Auxiliary inverters for xEV (HV compressor, HV pump, HV heater)

Industry

- Drives
- Energy storage systems
- Power converter
- Solar inverters
- Power supplies like UPS, isolated power supply
- SiC Power Modules



- Suitable for HV designs like **400 V/800 V**
- Increasing capacitance with DC bias and best in class capacitance density at operating point ($V_{op} + T_{op}$)
- Supports **miniaturization** with low inductive design

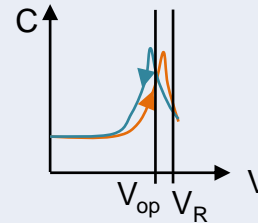
Basic facts

Qualification based on AECQ-200
Manufacturing site in EU (Deutschlandsberg, AT)
Quality management system according to IATF 16949:2016
Soldering Method: Reflow



Unique features

Innovative anti-ferroelectric ceramic material (positive bias behaviour)
High cooling efficiency due to high thermal conductivity
Good self-regulating properties



Resulting advantages

High capacitance density
High current capability
Low ESL (typ. 3 nH)
Low losses at high frequencies and high temperatures (up to +150 °C)
No limitation in dV/dt

→ **Ideal as snubber, filter cap and flying capacitor for SiC and GaN applications**



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